FIG. 1

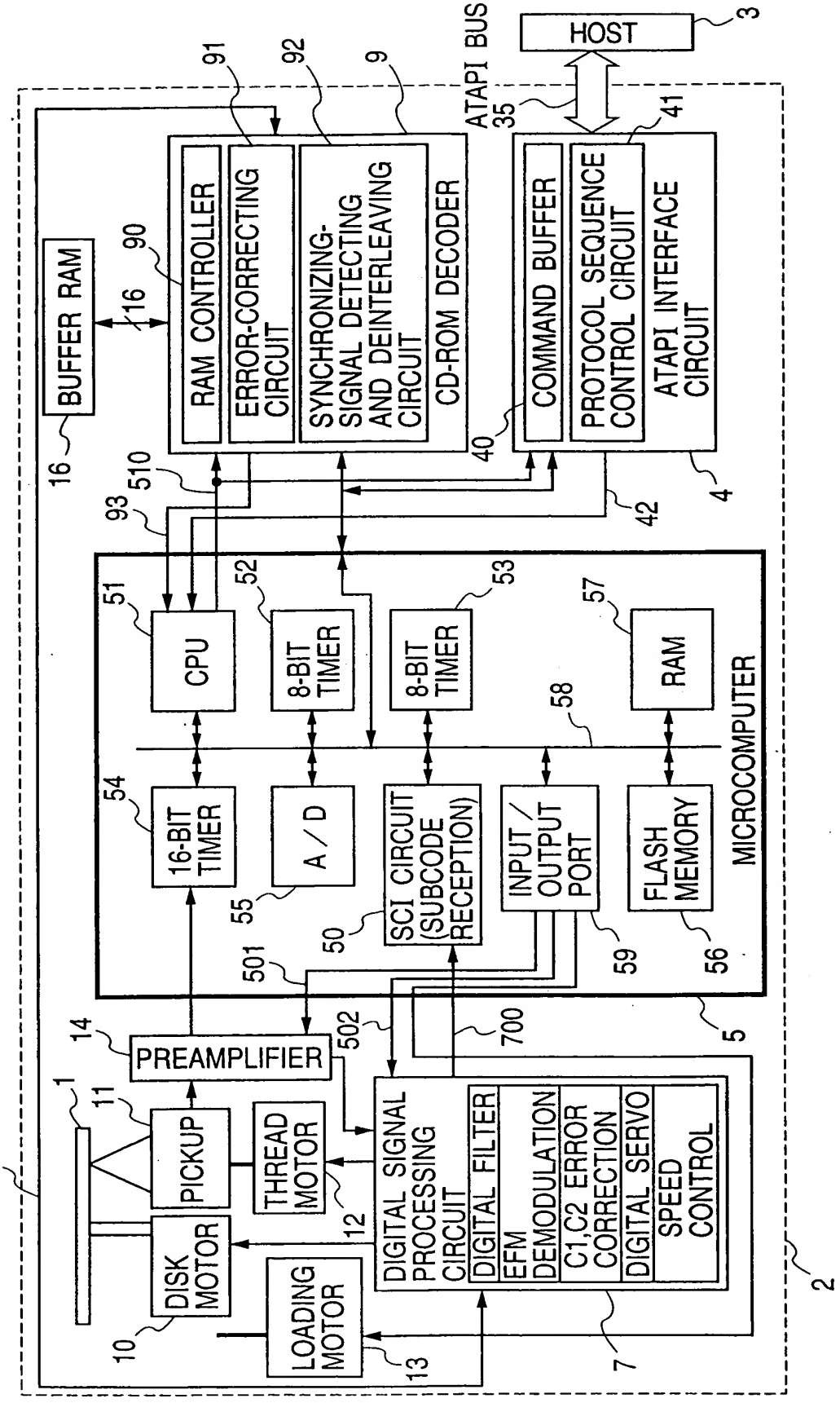

HOST
3
ATAPI BUS
35
41
91
92
9
90
16
BUFFER RAM
RAM CONTROLLER
ERROR-CORRECTING CIRCUIT
SYNCHRONIZING-SIGNAL DETECTING AND DEINTERLEAVING CIRCUIT
CD-ROM DECODER
COMMAND BUFFER
PROTOCOL SEQUENCE CONTROL CIRCUIT
ATAPI INTERFACE CIRCUIT
40
4
510
93
42
MICROCOMPUTER
CPU
51
8-BIT TIMER
52
8-BIT TIMER
53
RAM
57
58
16-BIT TIMER
54
A / D
55
SCI CIRCUIT (SUBCODE RECEPTION)
50
INPUT / OUTPUT PORT
59
FLASH MEMORY
56
501
5
PREAMPLIFIER
14
502
700
1
11
PICKUP
THREAD MOTOR
12
DIGITAL SIGNAL PROCESSING CIRCUIT
DIGITAL FILTER
EFM DEMODULATION
C1,C2 ERROR CORRECTION
DIGITAL SERVO
SPEED CONTROL
8
DISK MOTOR
10
LOADING MOTOR
13
7
2

FIG. 2

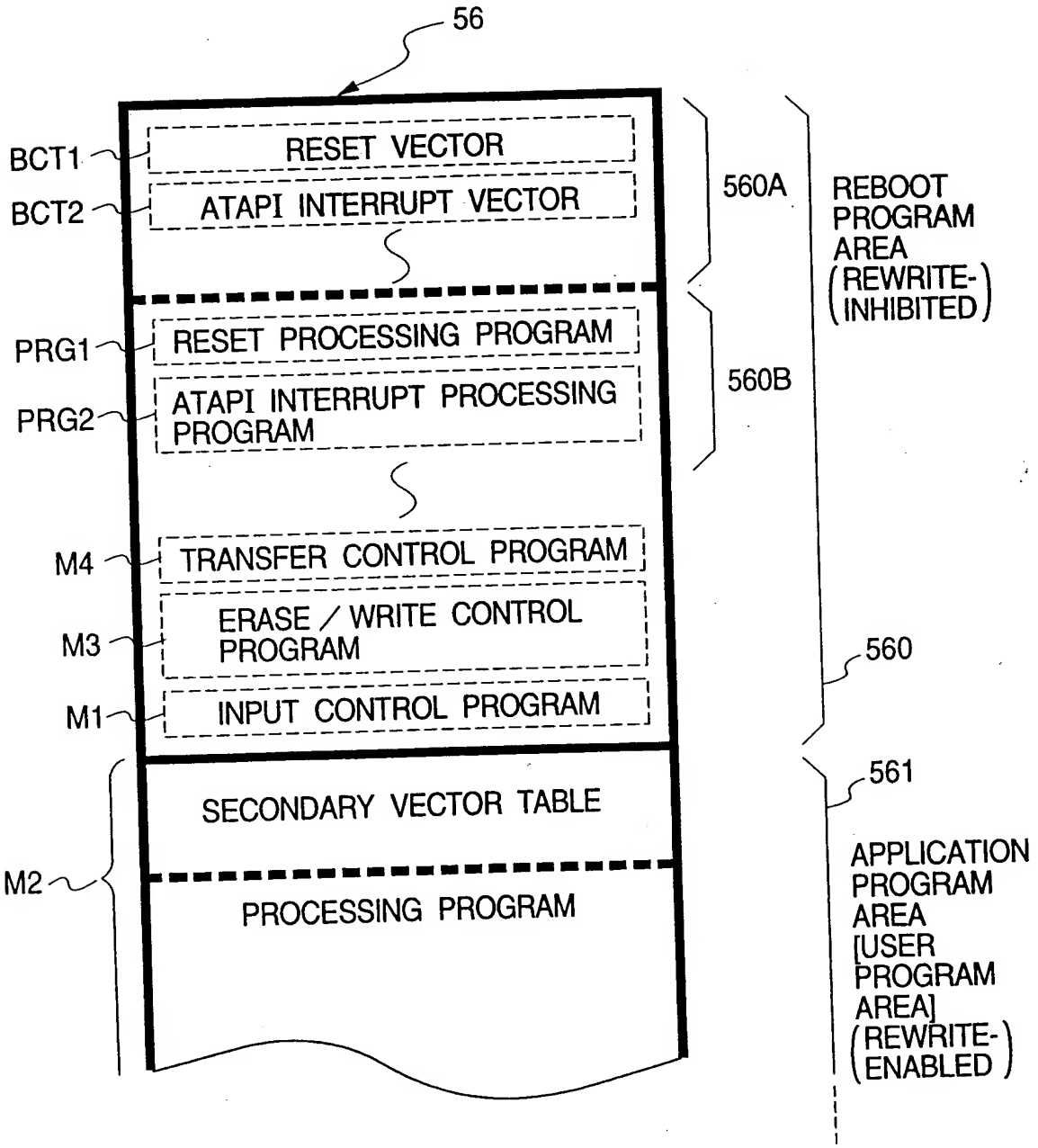

56
BCT1
RESET VECTOR
BCT2
ATAPI INTERRUPT VECTOR
560A
REBOOT PROGRAM AREA (REWRITE-INHIBITED)
PRG1
RESET PROCESSING PROGRAM
PRG2
ATAPI INTERRUPT PROCESSING PROGRAM
560B
M4
TRANSFER CONTROL PROGRAM
M3
ERASE / WRITE CONTROL PROGRAM
M1
INPUT CONTROL PROGRAM
560
561
SECONDARY VECTOR TABLE
M2
PROCESSING PROGRAM
APPLICATION PROGRAM AREA [USER PROGRAM AREA] (REWRITE-ENABLED)

FIG. 3

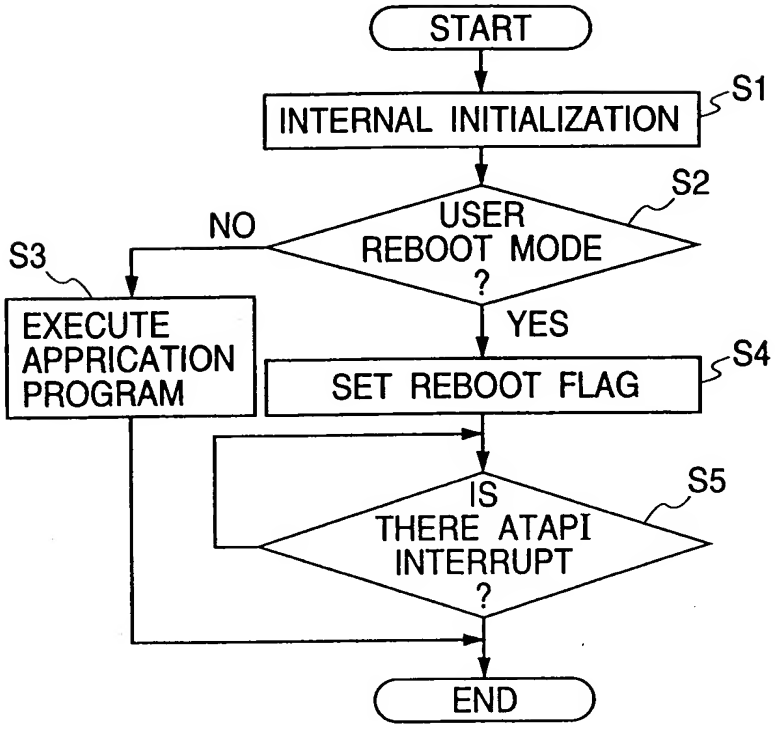

START
INTERNAL INITIALIZATION
S1
USER REBOOT MODE ?
S2
NO
S3
EXECUTE APPRICATION PROGRAM
YES
SET REBOOT FLAG
S4
IS THERE ATAPI INTERRUPT ?
S5
END

FIG. 4

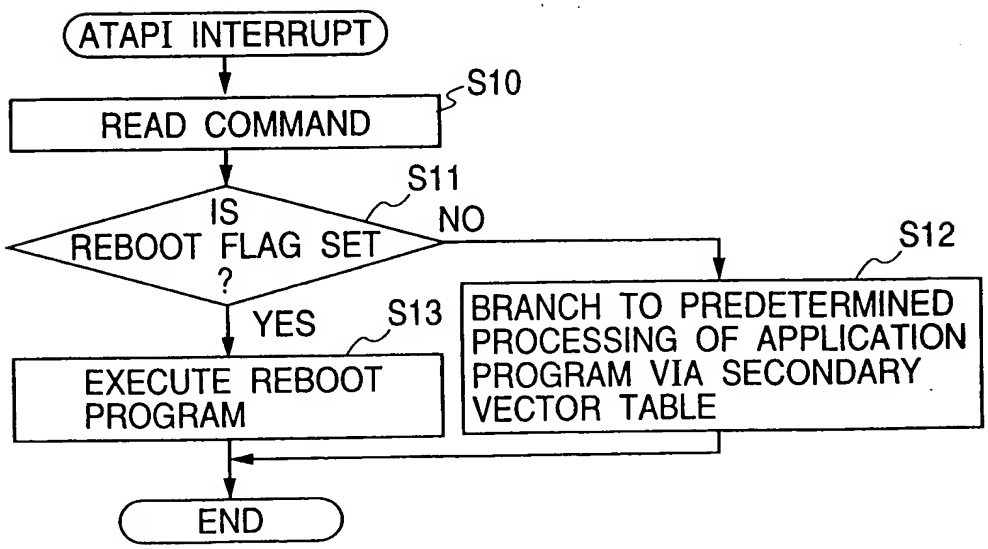

ATAPI INTERRUPT
READ COMMAND
S10
IS REBOOT FLAG SET ?
S11
NO
S12
YES
S13
EXECUTE REBOOT PROGRAM
BRANCH TO PREDETERMINED PROCESSING OF APPLICATION PROGRAM VIA SECONDARY VECTOR TABLE
END

FIG. 5

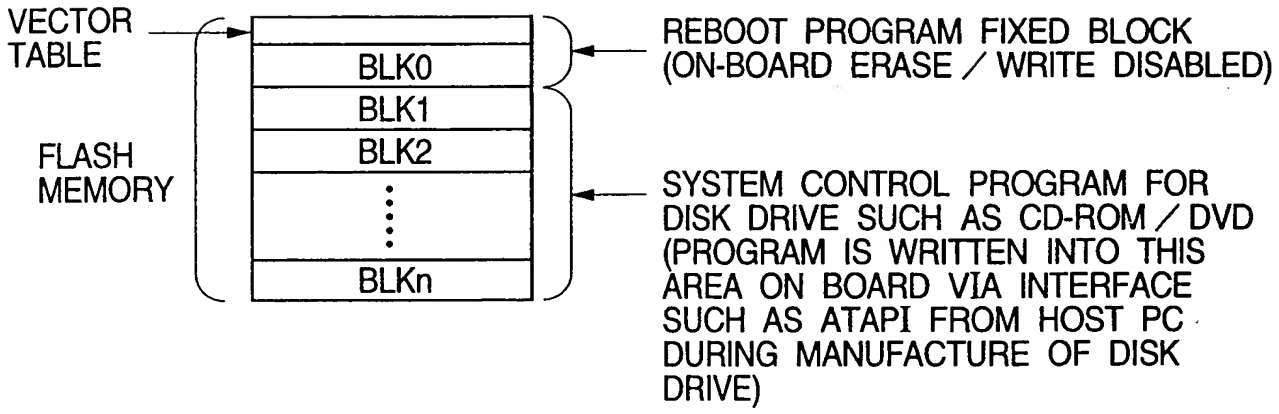

VECTOR TABLE
FLASH MEMORY
BLK0
BLK1
BLK2
BLKn
REBOOT PROGRAM FIXED BLOCK (ON-BOARD ERASE / WRITE DISABLED)
SYSTEM CONTROL PROGRAM FOR DISK DRIVE SUCH AS CD-ROM / DVD (PROGRAM IS WRITTEN INTO THIS AREA ON BOARD VIA INTERFACE SUCH AS ATAPI FROM HOST PC DURING MANUFACTURE OF DISK DRIVE)

FIG. 6

PROCESS OF MANUFACTURING MICROCOMPUTER HAVING BUILT-IN FLASH MEMORY

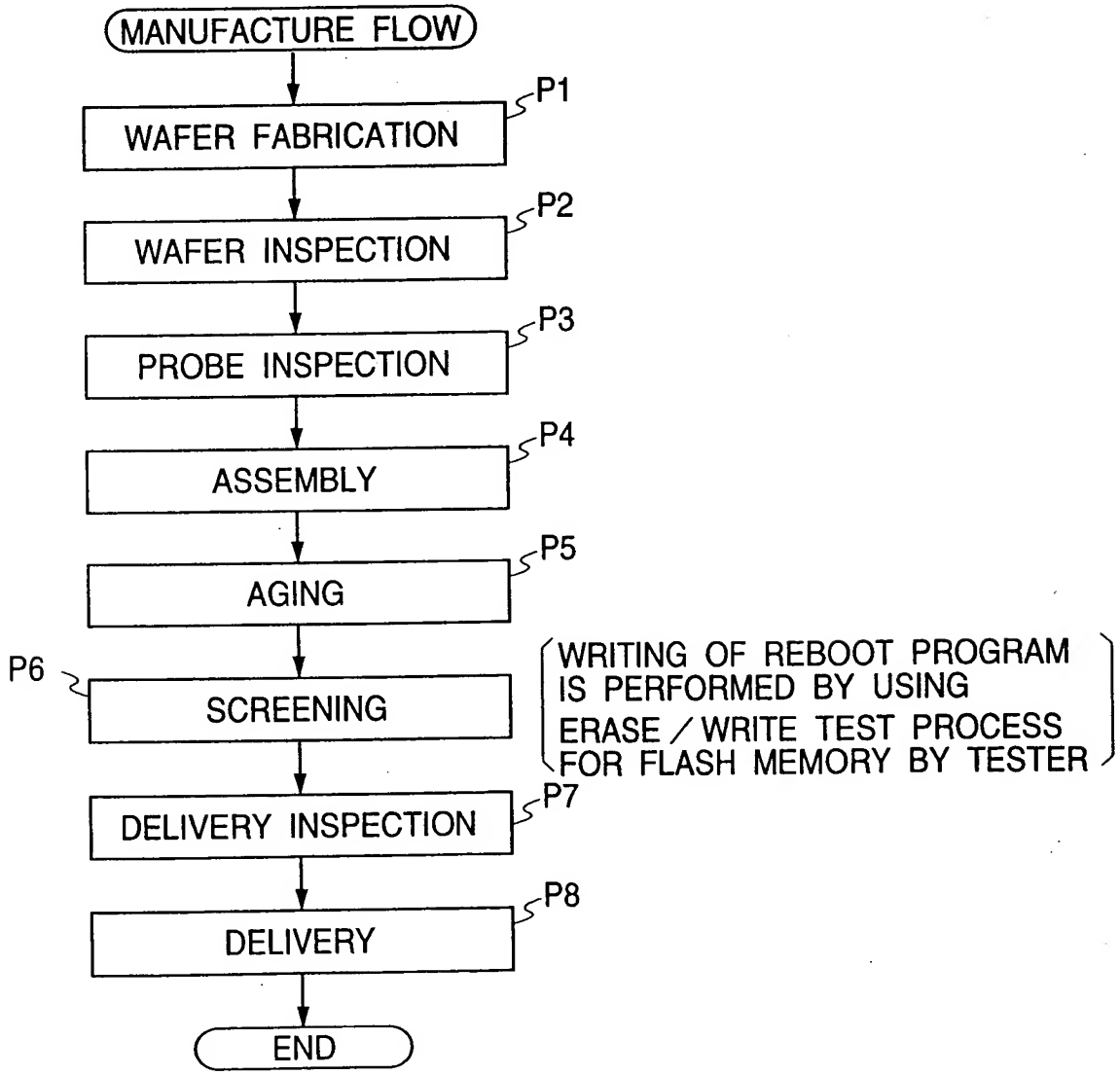


FIG. 7

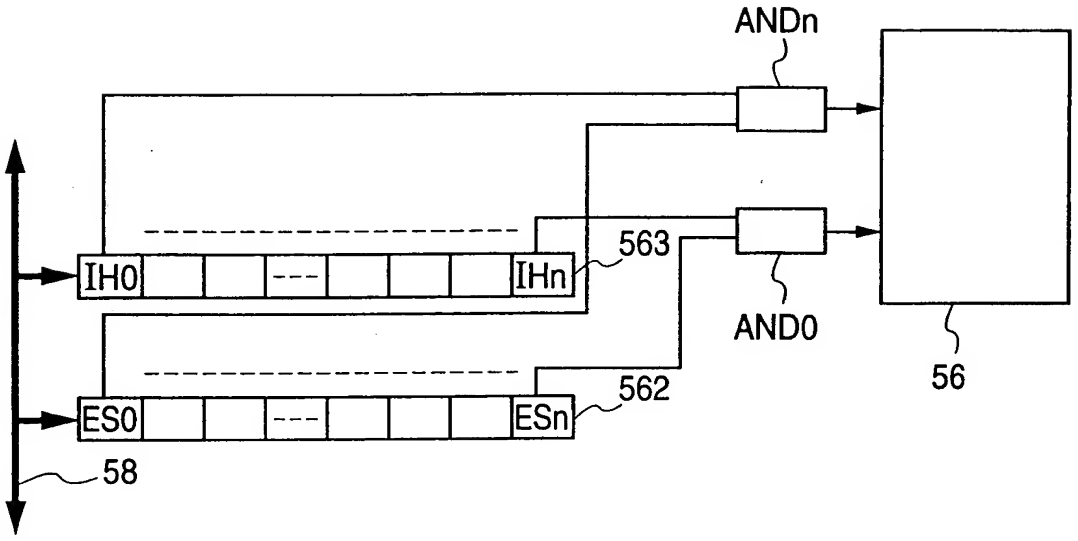

ANDn
IH0
IHn
563
AND0
56
ES0
ESn
562
58

FIG. 8

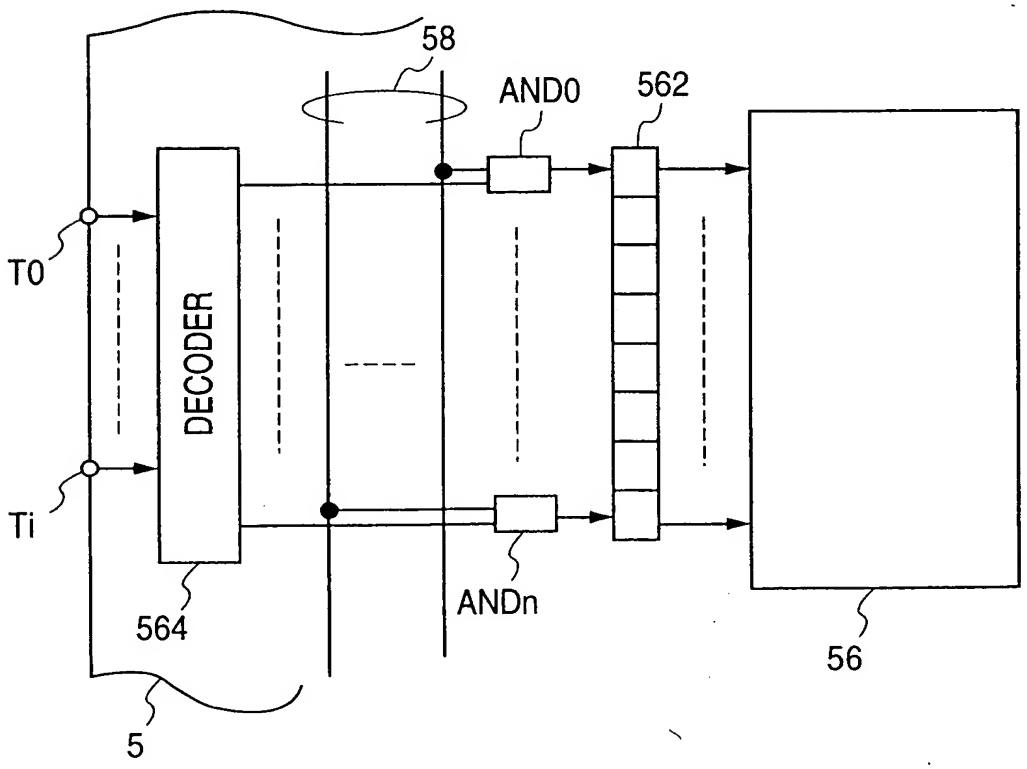

58
AND0
562
T0
DECODER
Ti
564
ANDn
56
5

FIG. 9

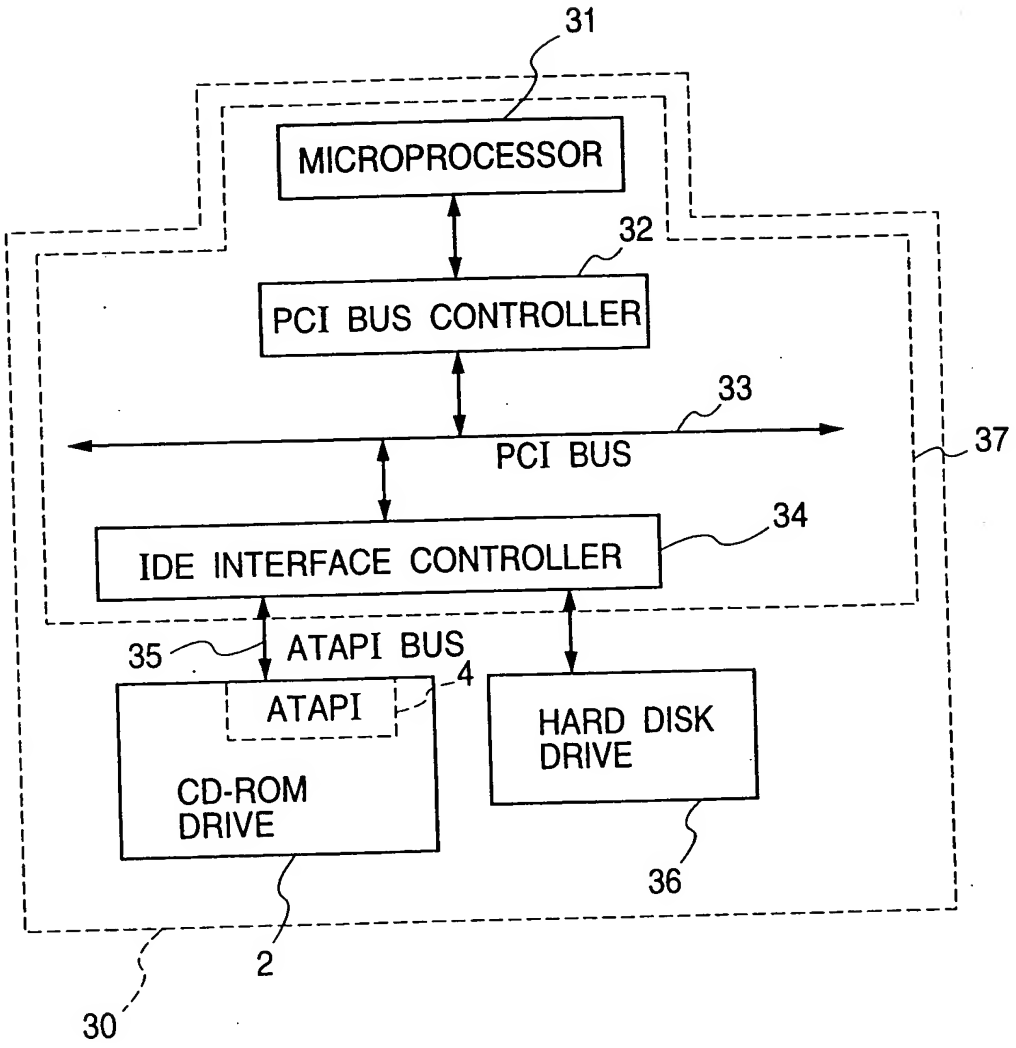

31
MICROPROCESSOR
32
PCI BUS CONTROLLER
33
PCI BUS
37
34
IDE INTERFACE CONTROLLER
35
ATAPI BUS
4
ATAPI
CD-ROM DRIVE
HARD DISK DRIVE
36
2
30

FIG. 10

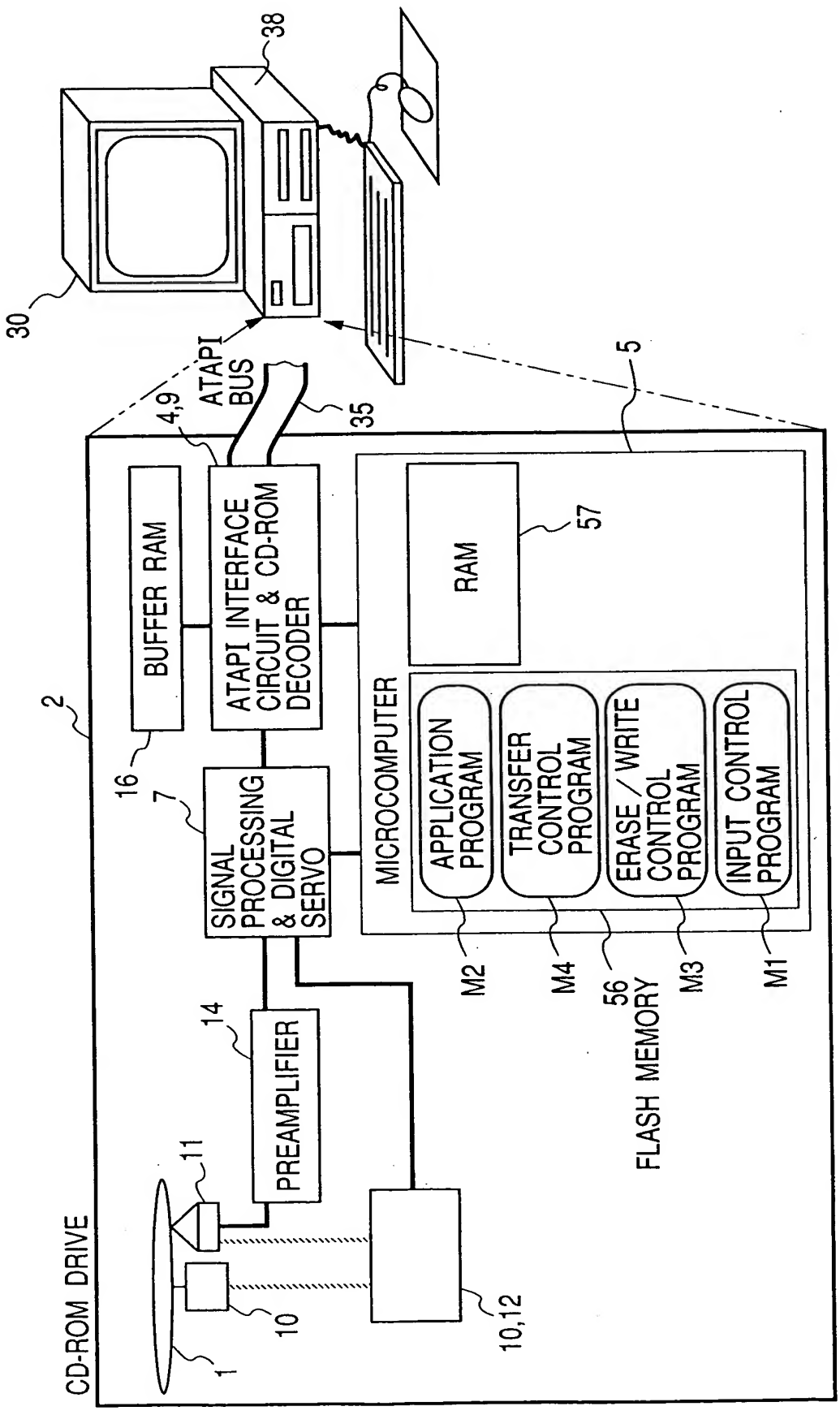

30
38
ATAPI BUS
4,9
35
5
2
CD-ROM DRIVE
BUFFER RAM
16
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
SIGNAL PROCESSING & DIGITAL SERVO
7
MICROCOMPUTER
RAM
57
APPLICATION PROGRAM
TRANSFER CONTROL PROGRAM
ERASE / WRITE CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
FLASH MEMORY
M3
M1
PREAMPLIFIER
14
11
1
10
10,12

FIG. 11

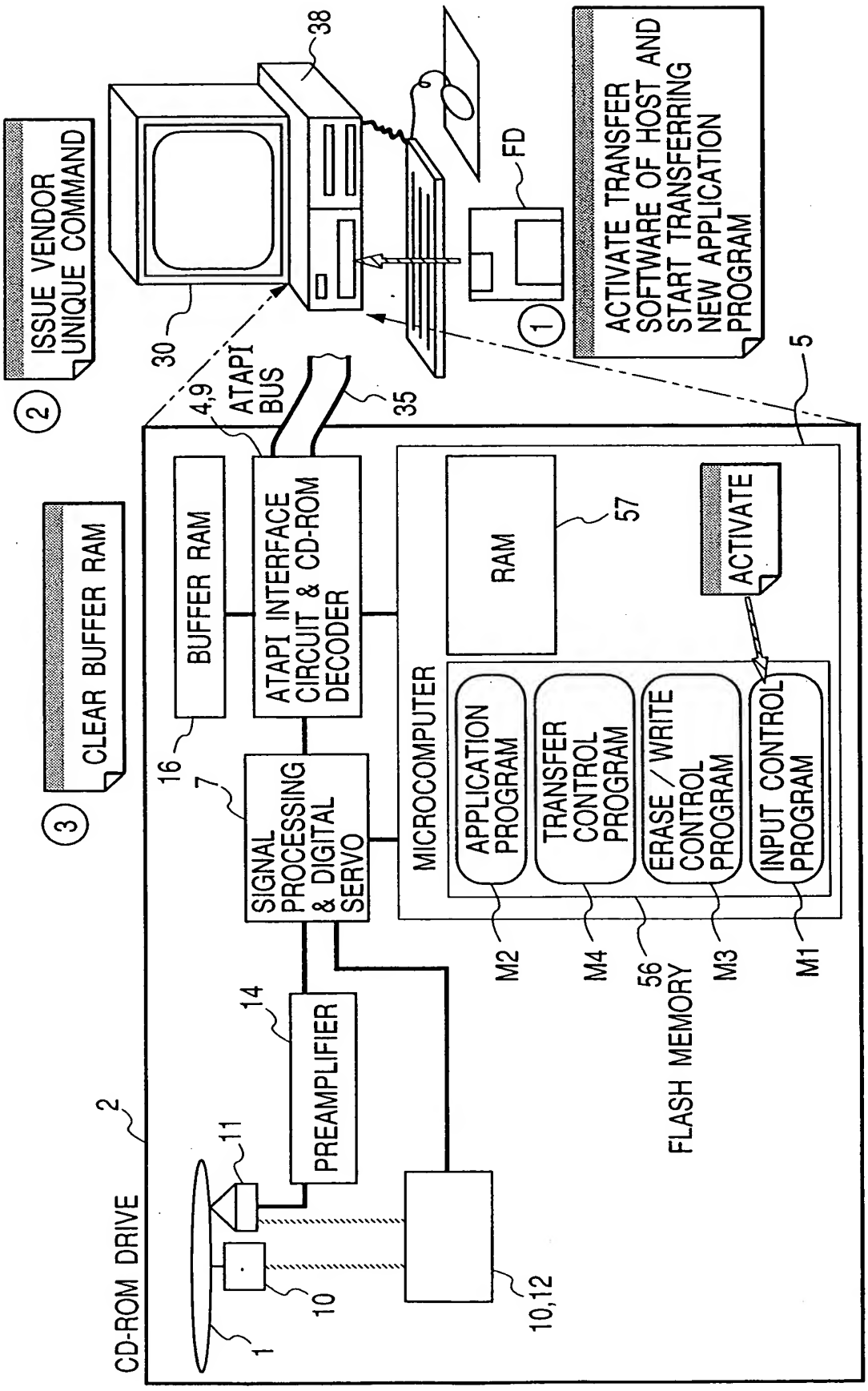

ACTIVATE TRANSFER SOFTWARE OF HOST AND START TRANSFERRING NEW APPLICATION PROGRAM
FD
38
30
ISSUE VENDOR UNIQUE COMMAND
ATAPI BUS
4,9
35
5
CLEAR BUFFER RAM
BUFFER RAM
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
RAM
57
ACTIVATE
MICROCOMPUTER
APPLICATION PROGRAM
TRANSFER CONTROL PROGRAM
ERASE / WRITE CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
M3
M1
FLASH MEMORY
16
7
SIGNAL PROCESSING & DIGITAL SERVO
14
PREAMPLIFIER
2
CD-ROM DRIVE
11
1
10
10,12

FIG. 12

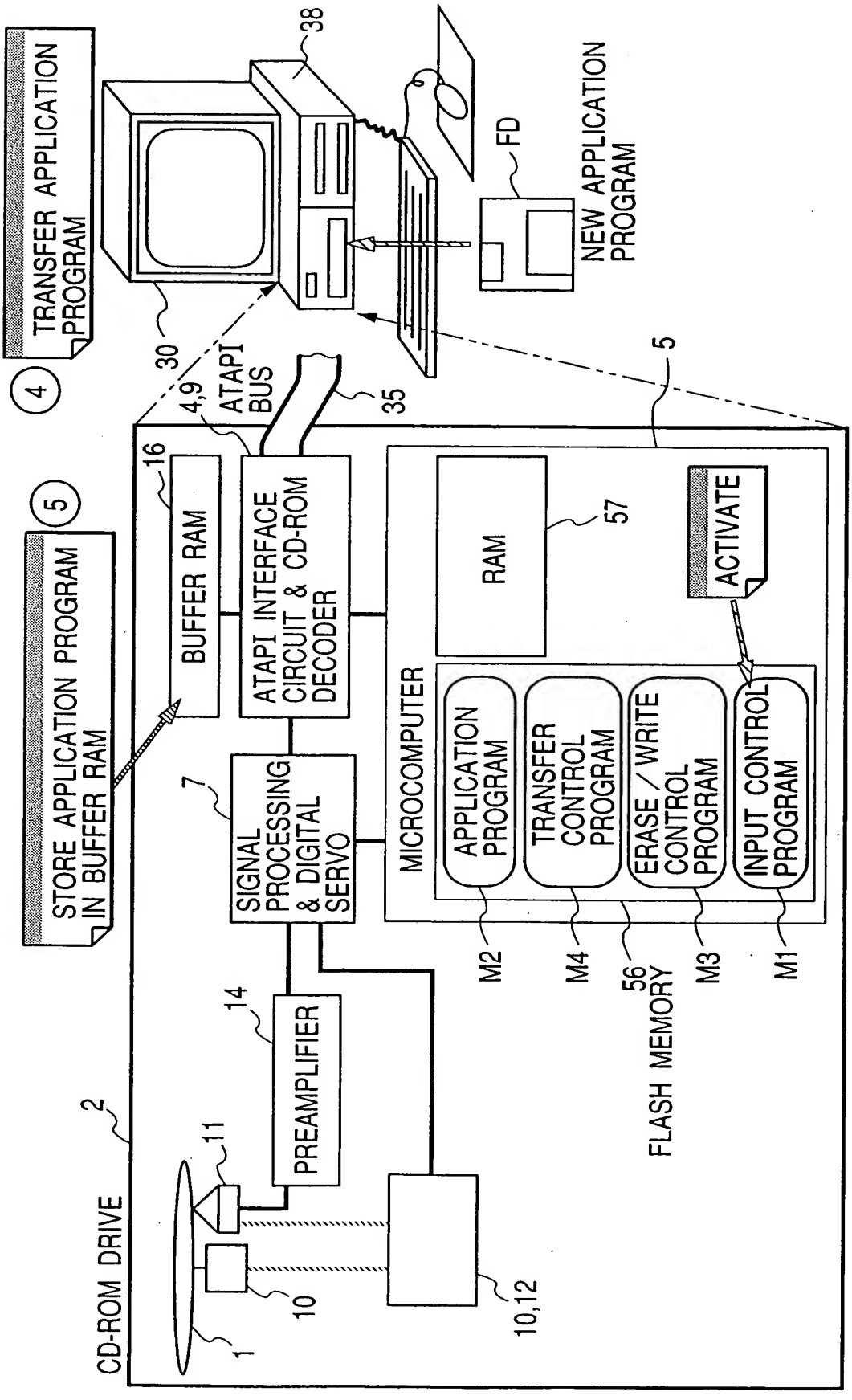

TRANSFER APPLICATION PROGRAM
4
38
FD
NEW APPLICATION PROGRAM
30
4,9
ATAPI BUS
35
5
STORE APPLICATION PROGRAM IN BUFFER RAM
5
16
BUFFER RAM
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
RAM
57
ACTIVATE
7
SIGNAL PROCESSING & DIGITAL SERVO
MICROCOMPUTER
APPLICATION PROGRAM
TRANSFER CONTROL PROGRAM
ERASE / WRITE CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
FLASH MEMORY
M3
M1
14
PREAMPLIFIER
2
CD-ROM DRIVE
11
10
1
10,12

FIG. 13

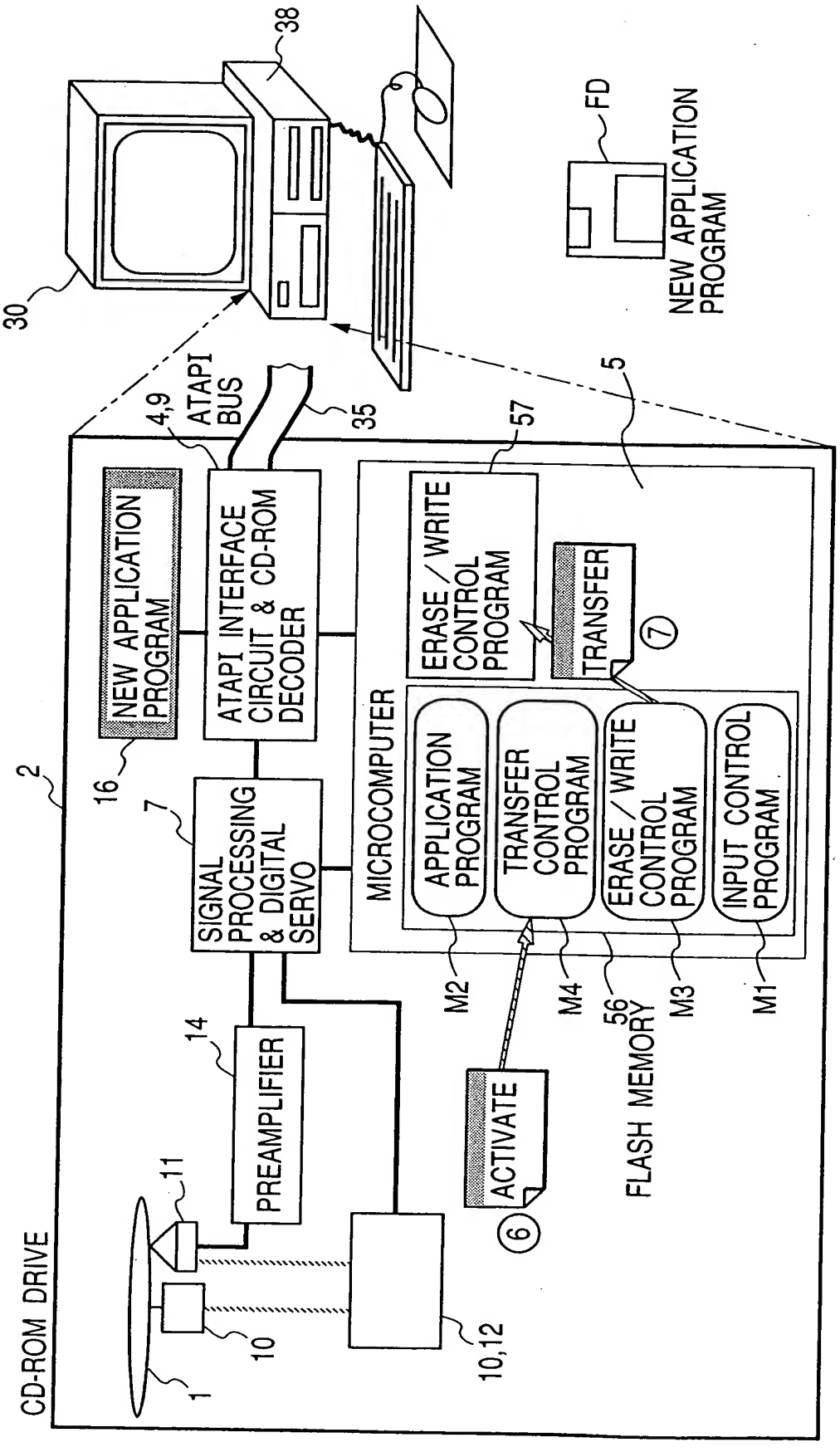

CD-ROM DRIVE
2
1
10
10,12
11
PREAMPLIFIER
14
SIGNAL PROCESSING & DIGITAL SERVO
7
NEW APPLICATION PROGRAM
16
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
4,9
ATAPI BUS
35
30
38
FD
NEW APPLICATION PROGRAM
5
MICROCOMPUTER
57
ERASE / WRITE CONTROL PROGRAM
TRANSFER
⑦
APPLICATION PROGRAM
TRANSFER CONTROL PROGRAM
ERASE / WRITE CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
M3
M1
FLASH MEMORY
ACTIVATE
⑥

FIG. 14

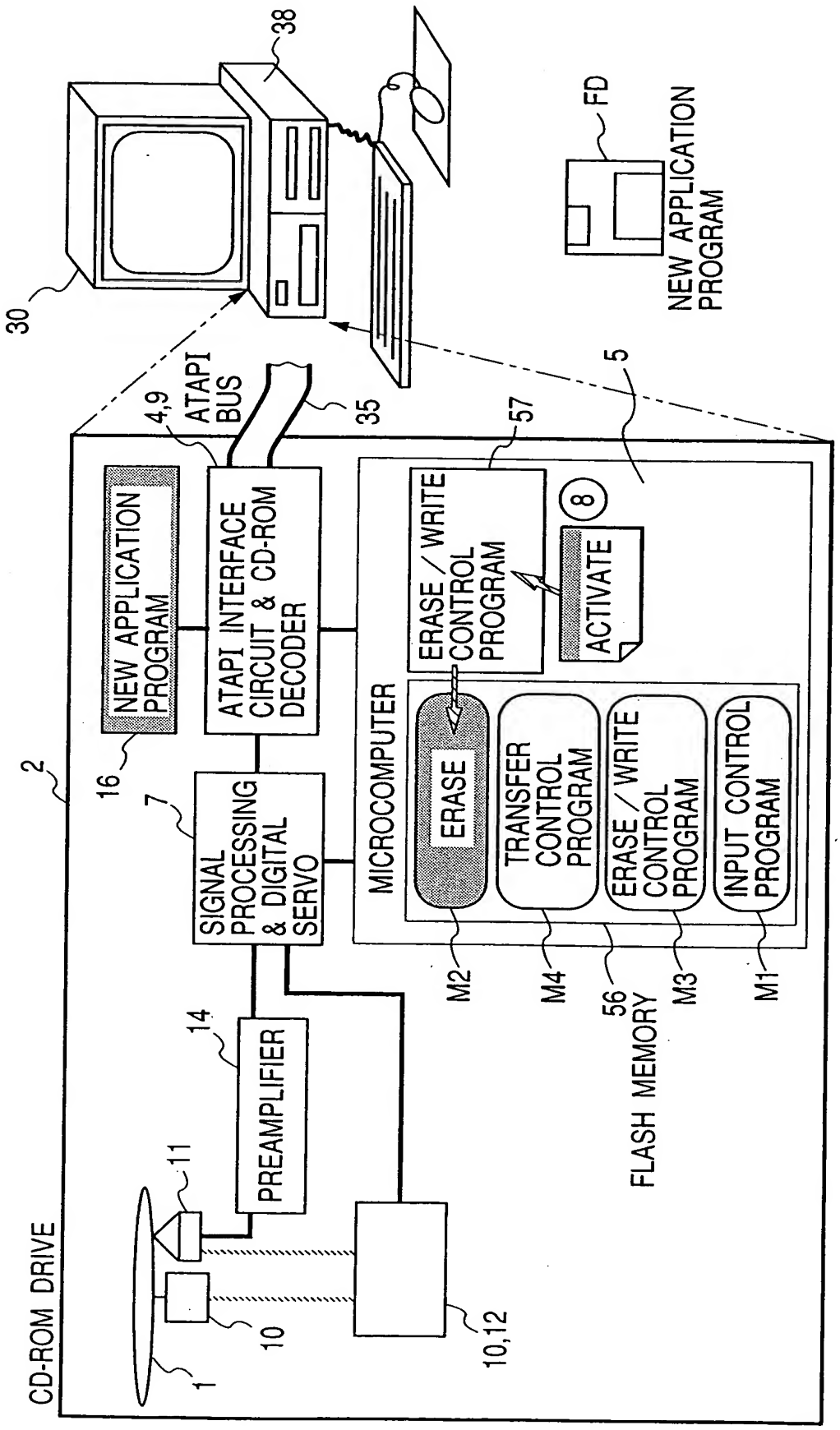

CD-ROM DRIVE
2
1
10
10,12
11
PREAMPLIFIER
14
SIGNAL PROCESSING & DIGITAL SERVO
7
16
NEW APPLICATION PROGRAM
4,9
ATAPI BUS
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
35
30
38
FD
NEW APPLICATION PROGRAM
5
57
MICROCOMPUTER
ERASE / WRITE CONTROL PROGRAM
ACTIVATE
8
ERASE
TRANSFER CONTROL PROGRAM
ERASE / WRITE CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
FLASH MEMORY
M3
M1

FIG. 15

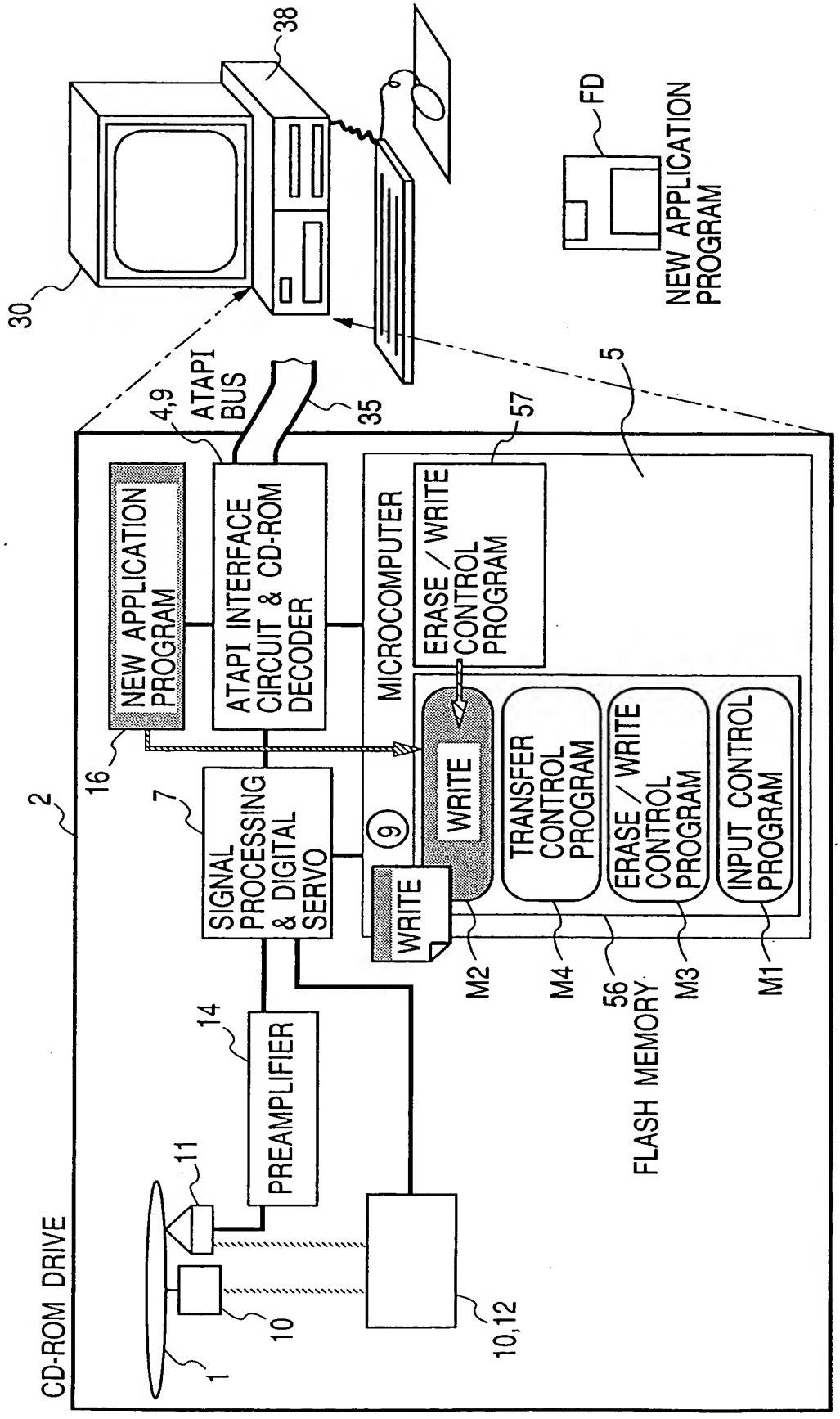

CD-ROM DRIVE
2
1
10
10,12
11
14
PREAMPLIFIER
7
SIGNAL PROCESSING & DIGITAL SERVO
16
NEW APPLICATION PROGRAM
4,9
ATAPI BUS
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
35
30
38
5
57
MICROCOMPUTER
ERASE / WRITE CONTROL PROGRAM
WRITE
TRANSFER CONTROL PROGRAM
ERASE / WRITE CONTROL PROGRAM
INPUT CONTROL PROGRAM
FLASH MEMORY
56
M1
M2
M3
M4
FD
NEW APPLICATION PROGRAM

FIG. 16

USER PROGRAM AREA REWRITING FLOWCHART

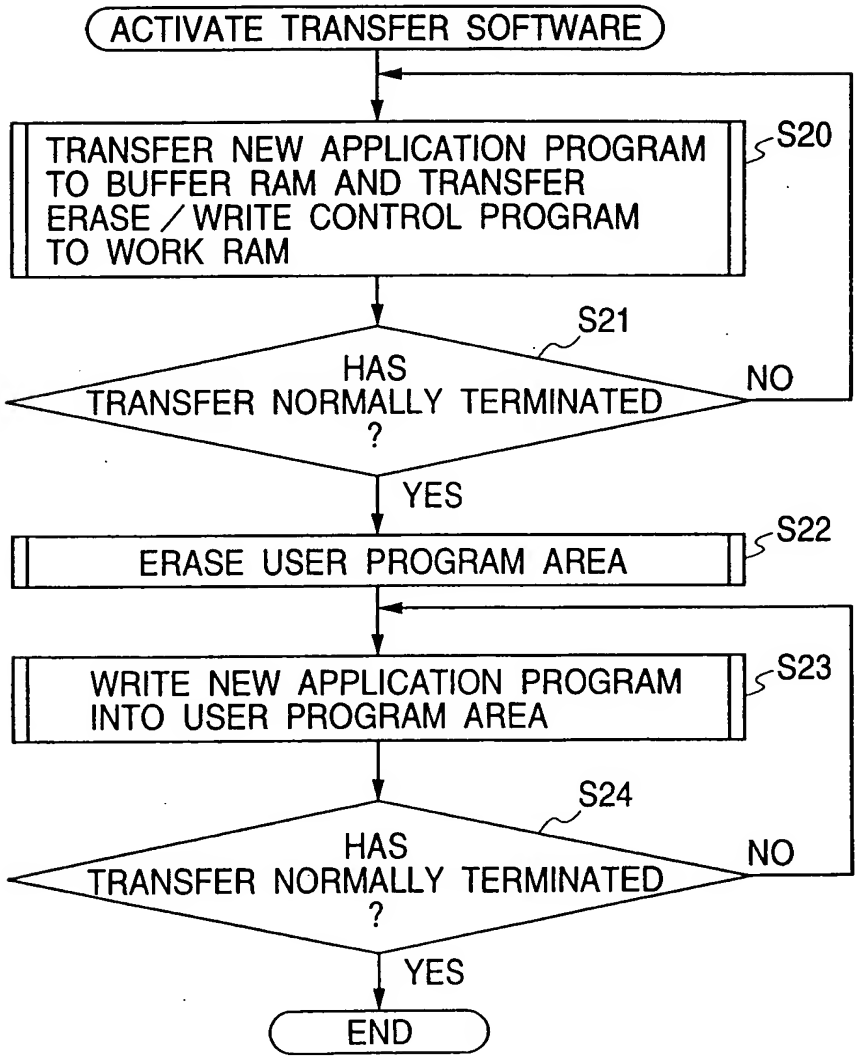


FIG. 17

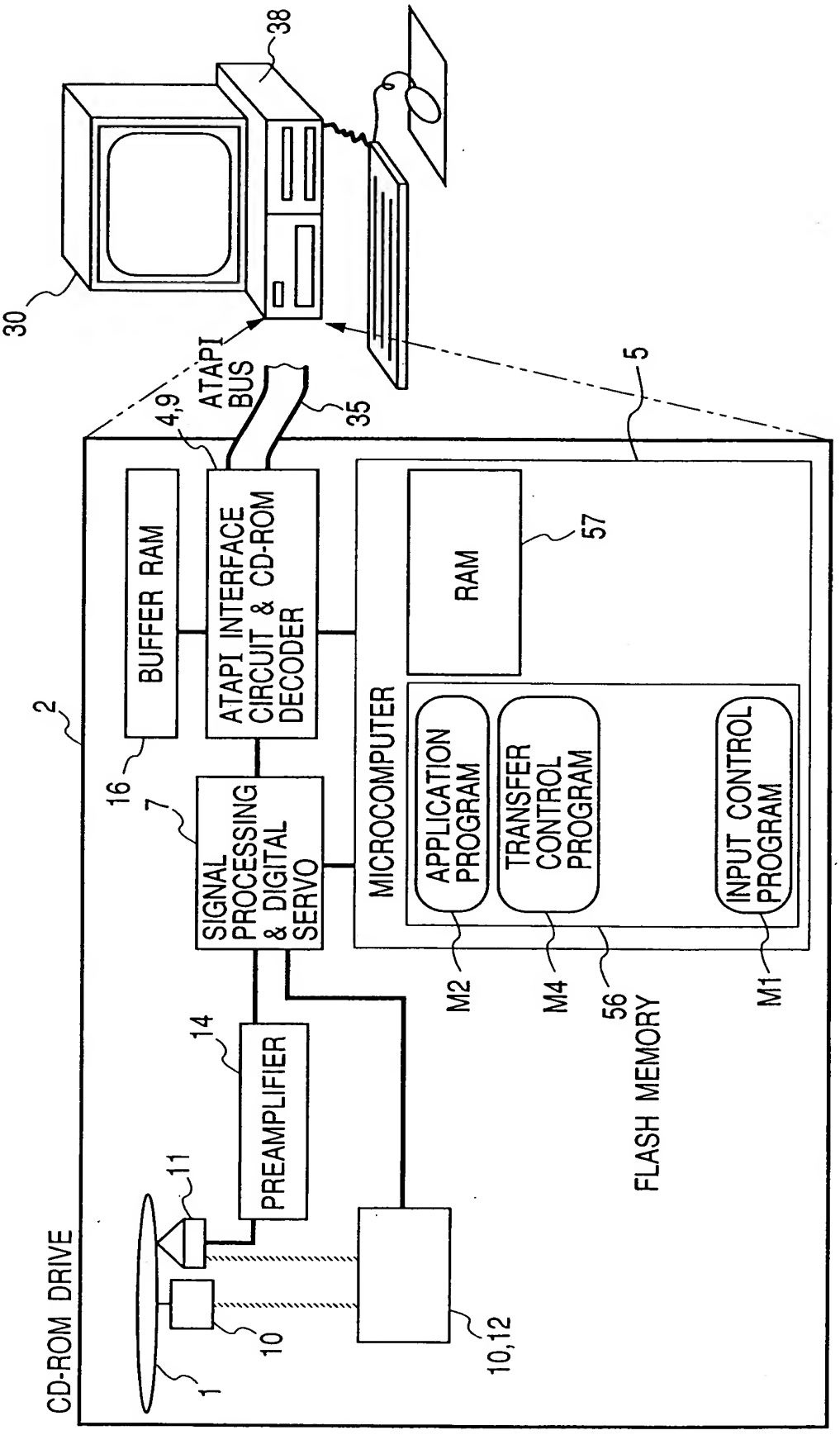

38
30
ATAPI BUS
35
4,9
5
2
BUFFER RAM
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
RAM
57
MICROCOMPUTER
APPLICATION PROGRAM
TRANSFER CONTROL PROGRAM
INPUT CONTROL PROGRAM
16
7
SIGNAL PROCESSING & DIGITAL SERVO
14
PREAMPLIFIER
11
CD-ROM DRIVE
1
10
10,12
M2
M4
56
M1
FLASH MEMORY

FIG. 18

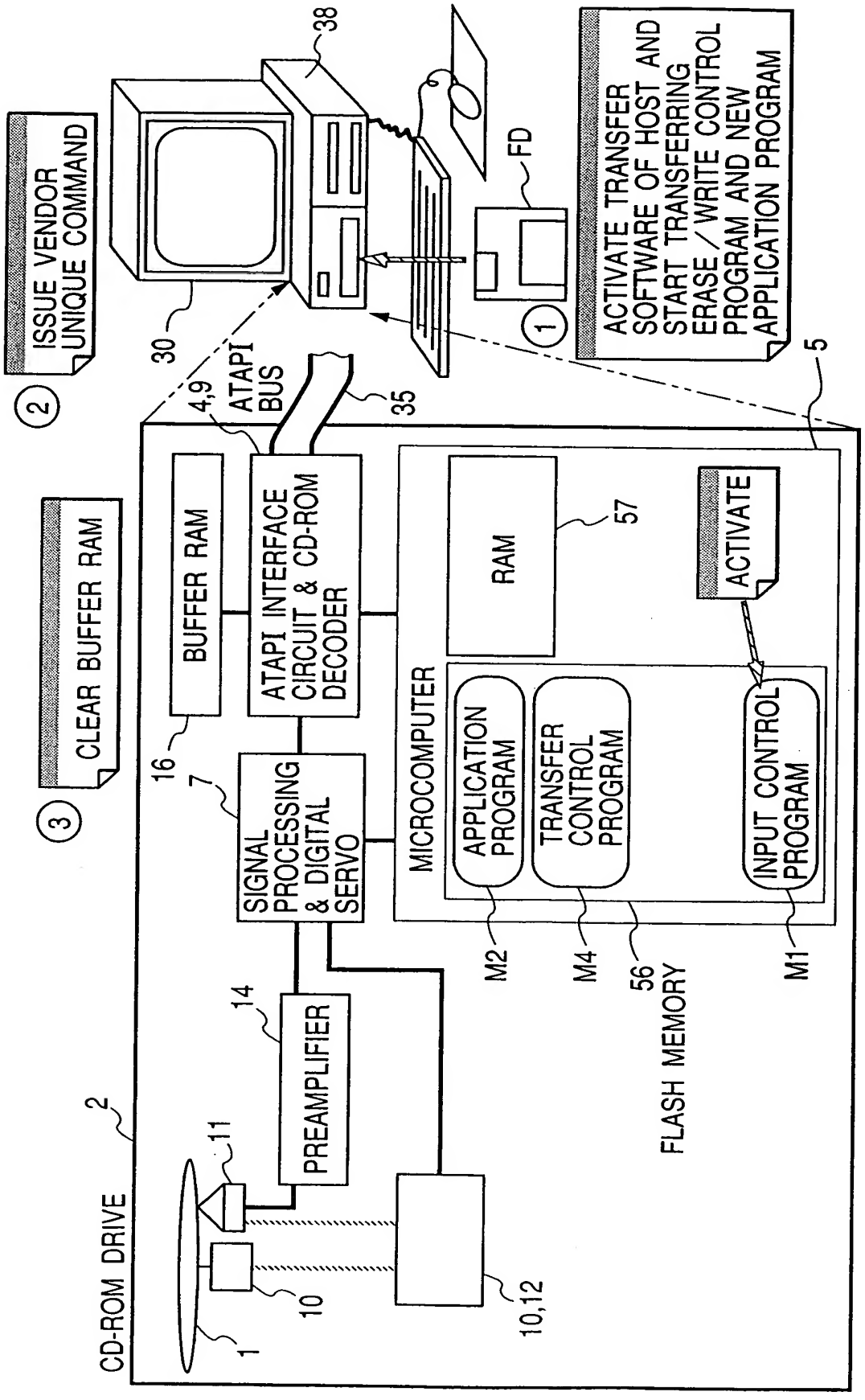

ACTIVATE TRANSFER SOFTWARE OF HOST AND START TRANSFERRING ERASE / WRITE CONTROL PROGRAM AND NEW APPLICATION PROGRAM
ISSUE VENDOR UNIQUE COMMAND
CLEAR BUFFER RAM
FD
38
30
4,9
ATAPI BUS
35
5
BUFFER RAM
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
RAM
57
ACTIVATE
MICROCOMPUTER
APPLICATION PROGRAM
TRANSFER CONTROL PROGRAM
INPUT CONTROL PROGRAM
16
7
SIGNAL PROCESSING & DIGITAL SERVO
14
PREAMPLIFIER
11
2
CD-ROM DRIVE
1
10
10,12
M2
M4
56
FLASH MEMORY
M1

FIG. 19

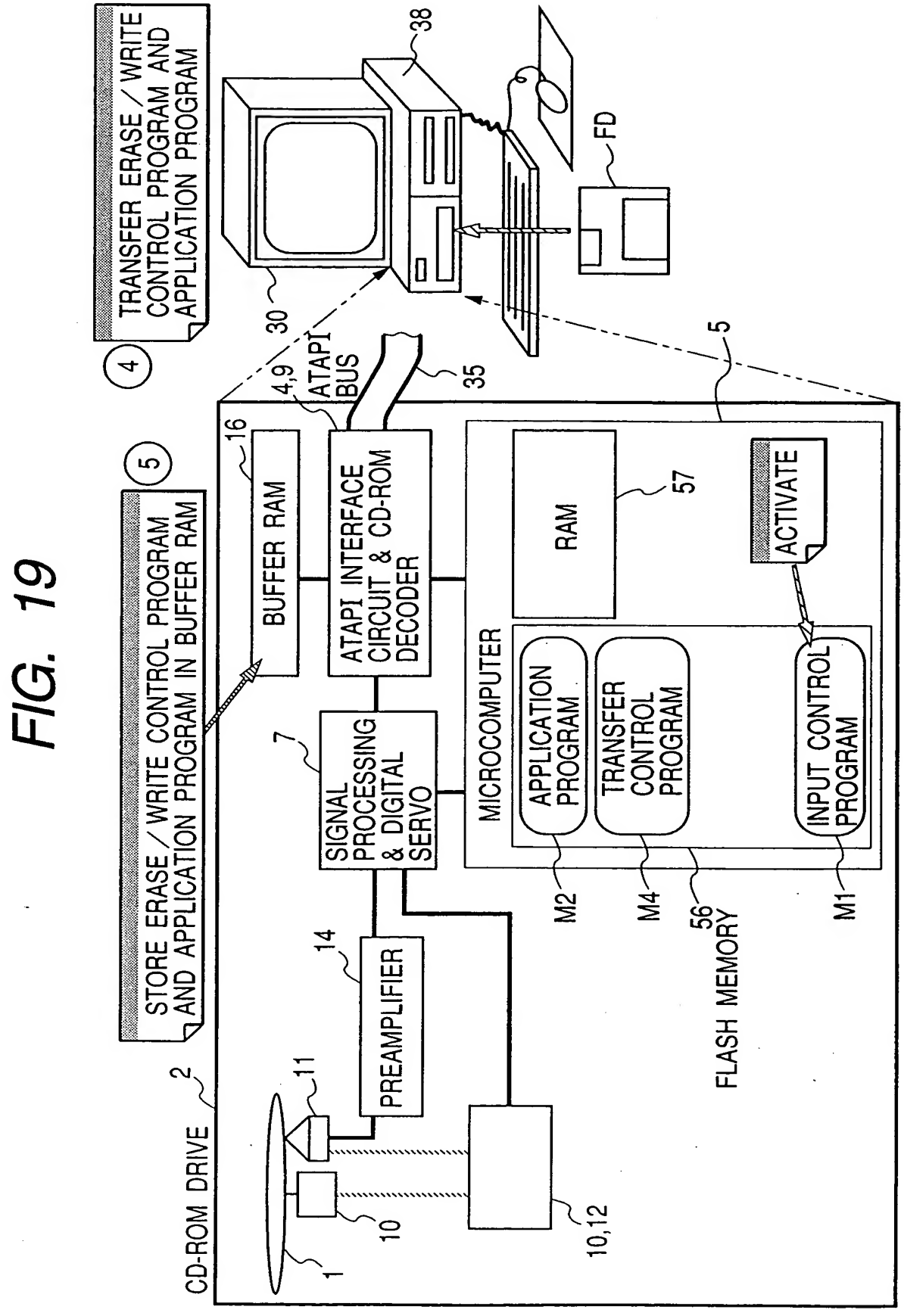

4
TRANSFER ERASE / WRITE CONTROL PROGRAM AND APPLICATION PROGRAM
38
FD
30
4,9
ATAPI BUS
35
5
5
STORE ERASE / WRITE CONTROL PROGRAM AND APPLICATION PROGRAM IN BUFFER RAM
16
BUFFER RAM
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
RAM
57
ACTIVATE
MICROCOMPUTER
7
SIGNAL PROCESSING & DIGITAL SERVO
APPLICATION PROGRAM
TRANSFER CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
FLASH MEMORY
M1
14
PREAMPLIFIER
2
CD-ROM DRIVE
11
1
10
10,12

FIG. 20

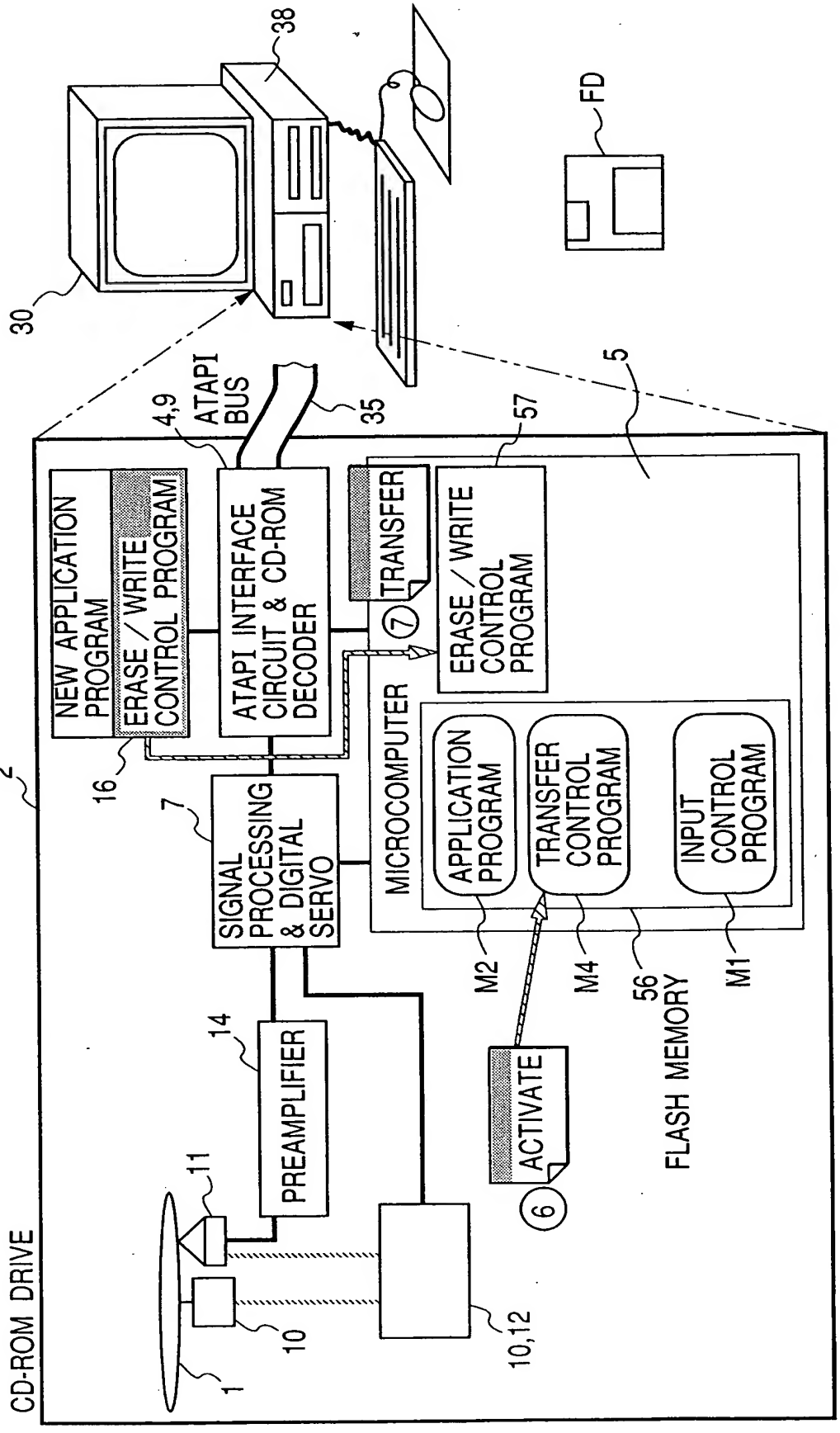

38
FD
30
5
4,9
ATAPI BUS
35
57
NEW APPLICATION PROGRAM
ERASE / WRITE CONTROL PROGRAM
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
TRANSFER
ERASE / WRITE CONTROL PROGRAM
2
16
7
SIGNAL PROCESSING & DIGITAL SERVO
MICROCOMPUTER
APPLICATION PROGRAM
TRANSFER CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
M1
FLASH MEMORY
14
PREAMPLIFIER
11
ACTIVATE
CD-ROM DRIVE
10
10,12
1

FIG. 21

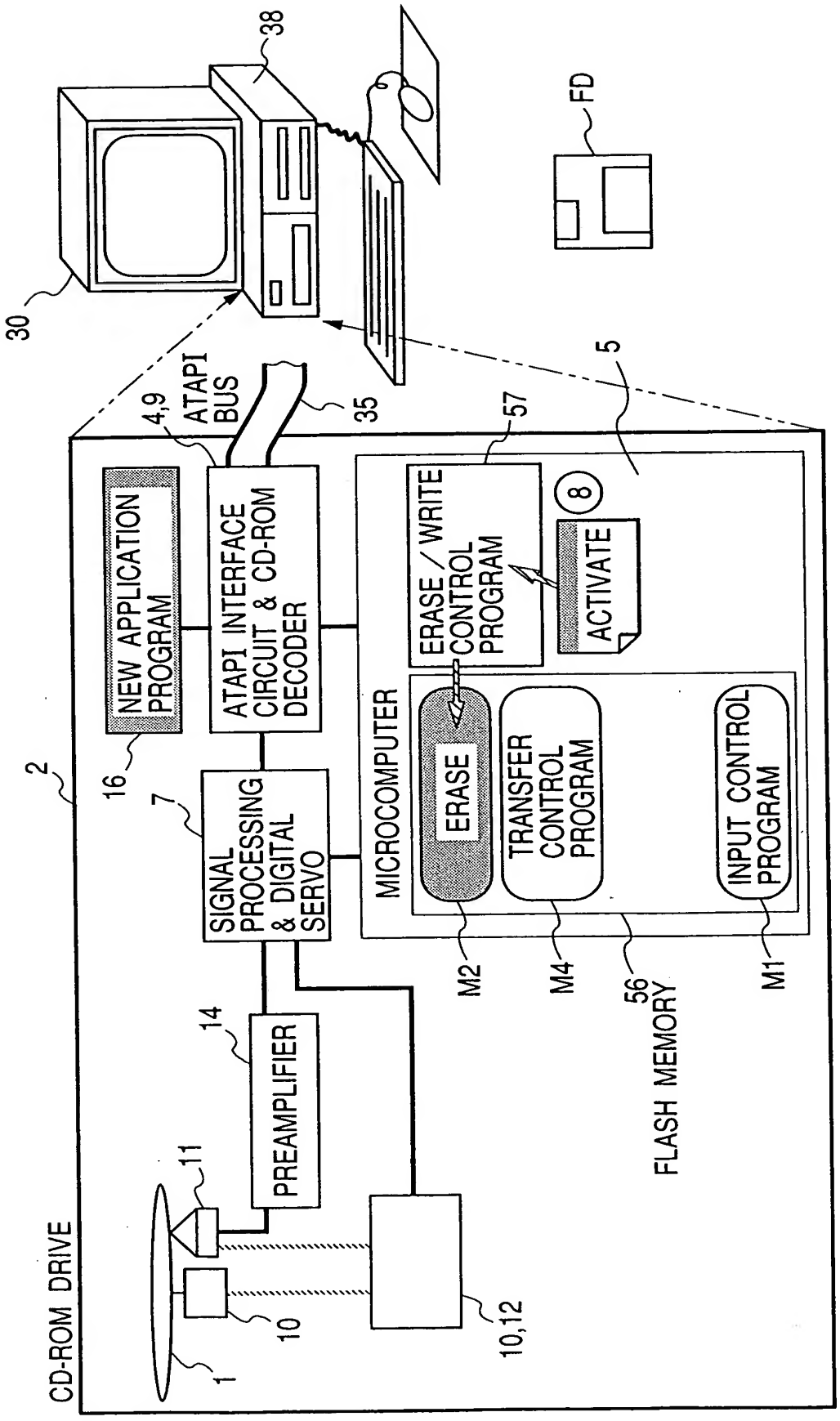

38
FD
30
5
ATAPI BUS
4,9
35
57
NEW APPLICATION PROGRAM
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
ERASE / WRITE CONTROL PROGRAM
8
ACTIVATE
2
16
7
SIGNAL PROCESSING & DIGITAL SERVO
MICROCOMPUTER
ERASE
TRANSFER CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
FLASH MEMORY
M1
14
PREAMPLIFIER
11
CD-ROM DRIVE
10
1
10,12

FIG. 22

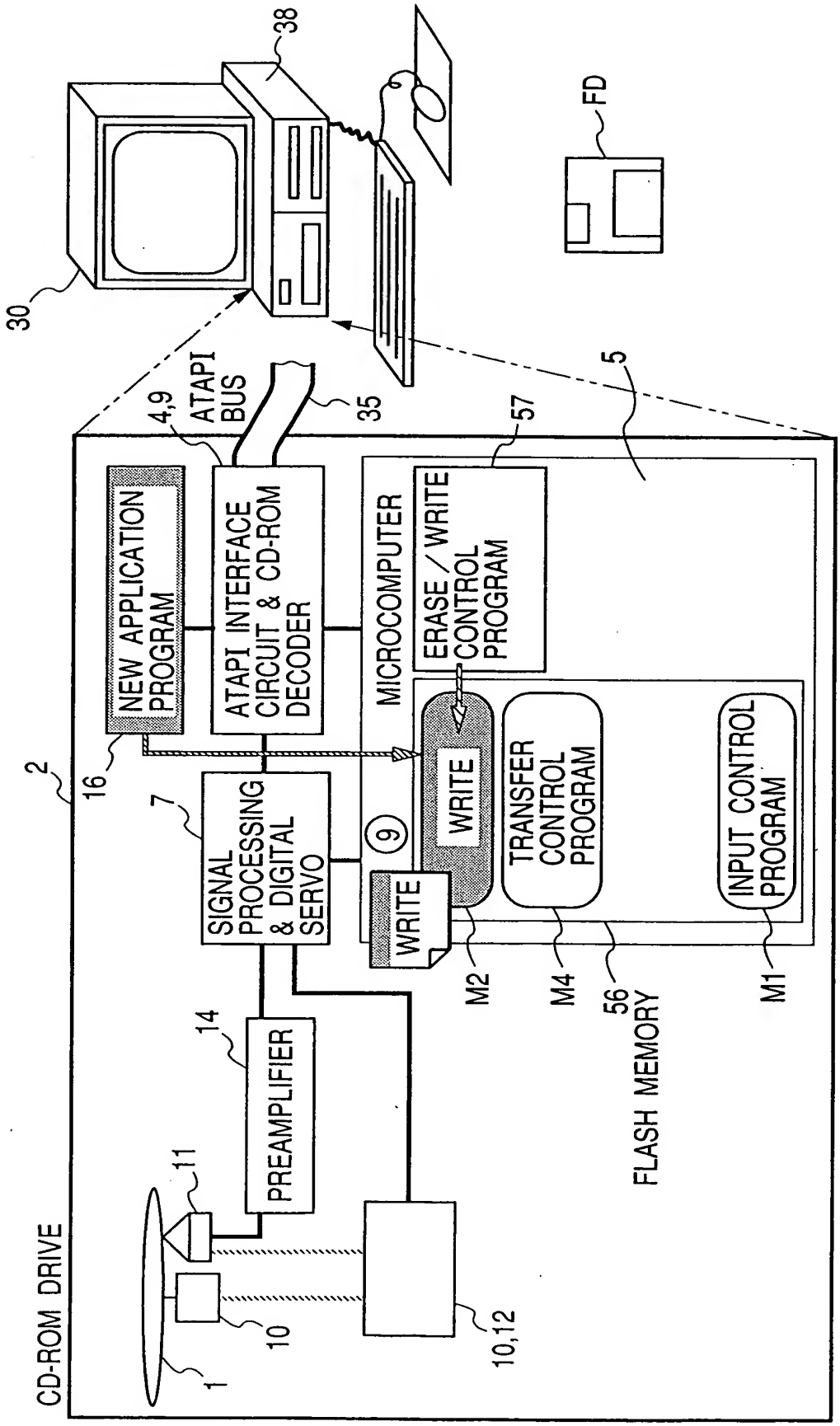

38
FD
30
4,9
ATAPI BUS
35
5
57
NEW APPLICATION PROGRAM
ATAPI INTERFACE CIRCUIT & CD-ROM DECODER
MICROCOMPUTER
ERASE / WRITE CONTROL PROGRAM
2
16
7
SIGNAL PROCESSING & DIGITAL SERVO
9
WRITE
WRITE
TRANSFER CONTROL PROGRAM
INPUT CONTROL PROGRAM
M2
M4
56
M1
FLASH MEMORY
14
PREAMPLIFIER
11
CD-ROM DRIVE
1
10
10,12

FIG. 23

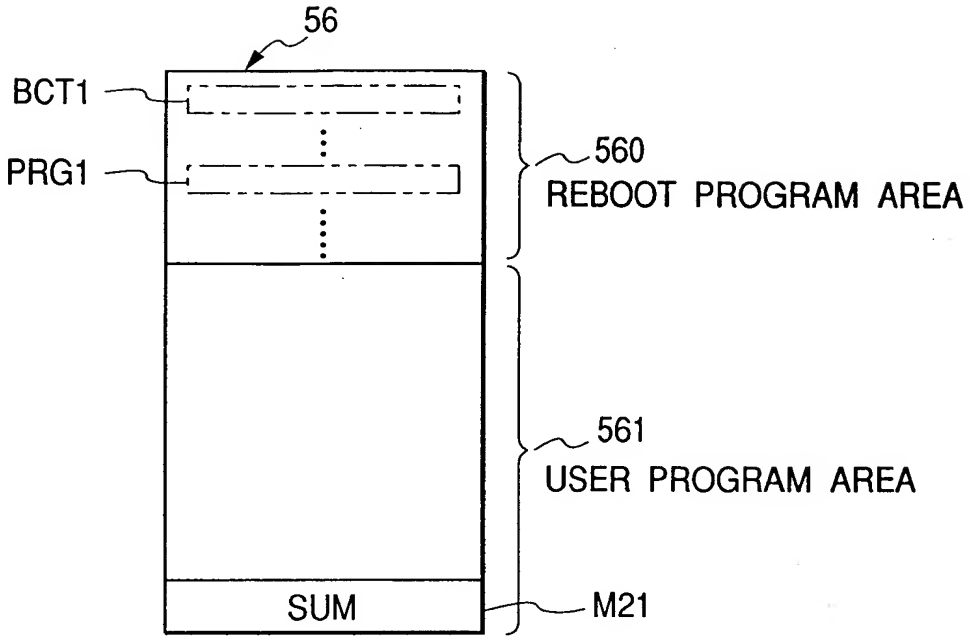

56
BCT1
PRG1
560
REBOOT PROGRAM AREA
561
USER PROGRAM AREA
SUM
M21

FIG. 25

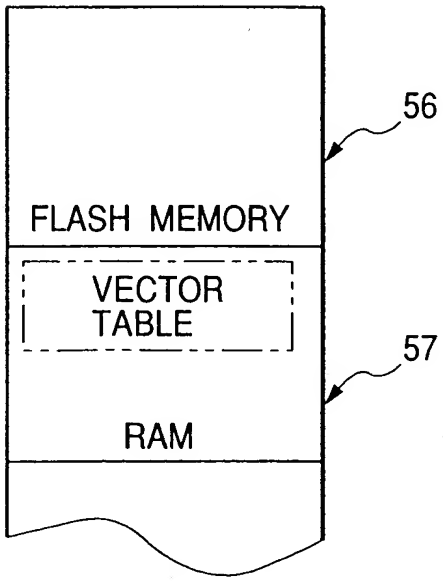

56
FLASH MEMORY
VECTOR TABLE
57
RAM

FIG. 24

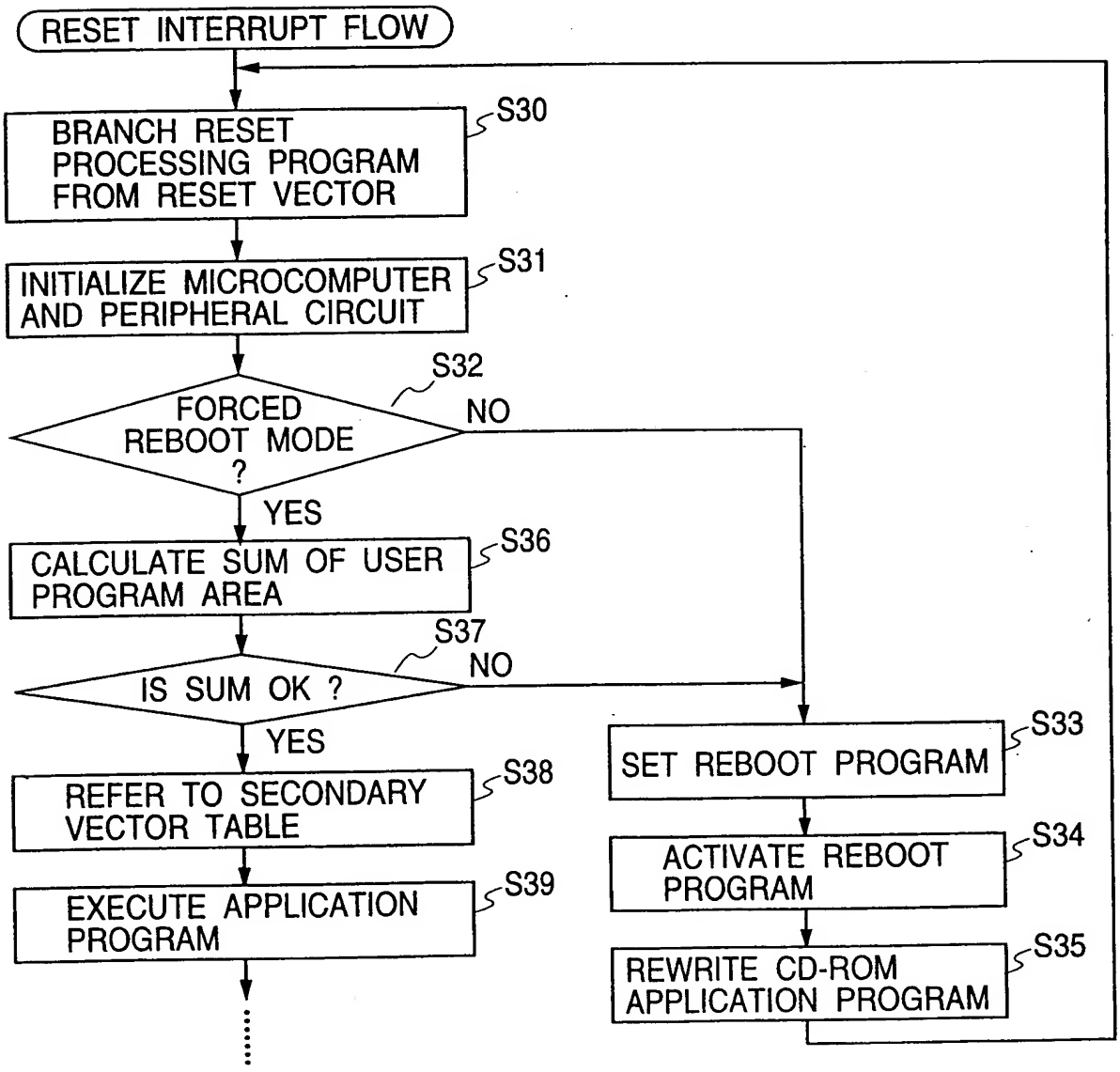

RESET INTERRUPT FLOW
BRANCH RESET PROCESSING PROGRAM FROM RESET VECTOR
S30
INITIALIZE MICROCOMPUTER AND PERIPHERAL CIRCUIT
S31
FORCED REBOOT MODE ?
S32
NO
YES
CALCULATE SUM OF USER PROGRAM AREA
S36
IS SUM OK ?
S37
NO
YES
REFER TO SECONDARY VECTOR TABLE
S38
EXECUTE APPLICATION PROGRAM
S39
SET REBOOT PROGRAM
S33
ACTIVATE REBOOT PROGRAM
S34
REWRITE CD-ROM APPLICATION PROGRAM
S35

FIG. 26

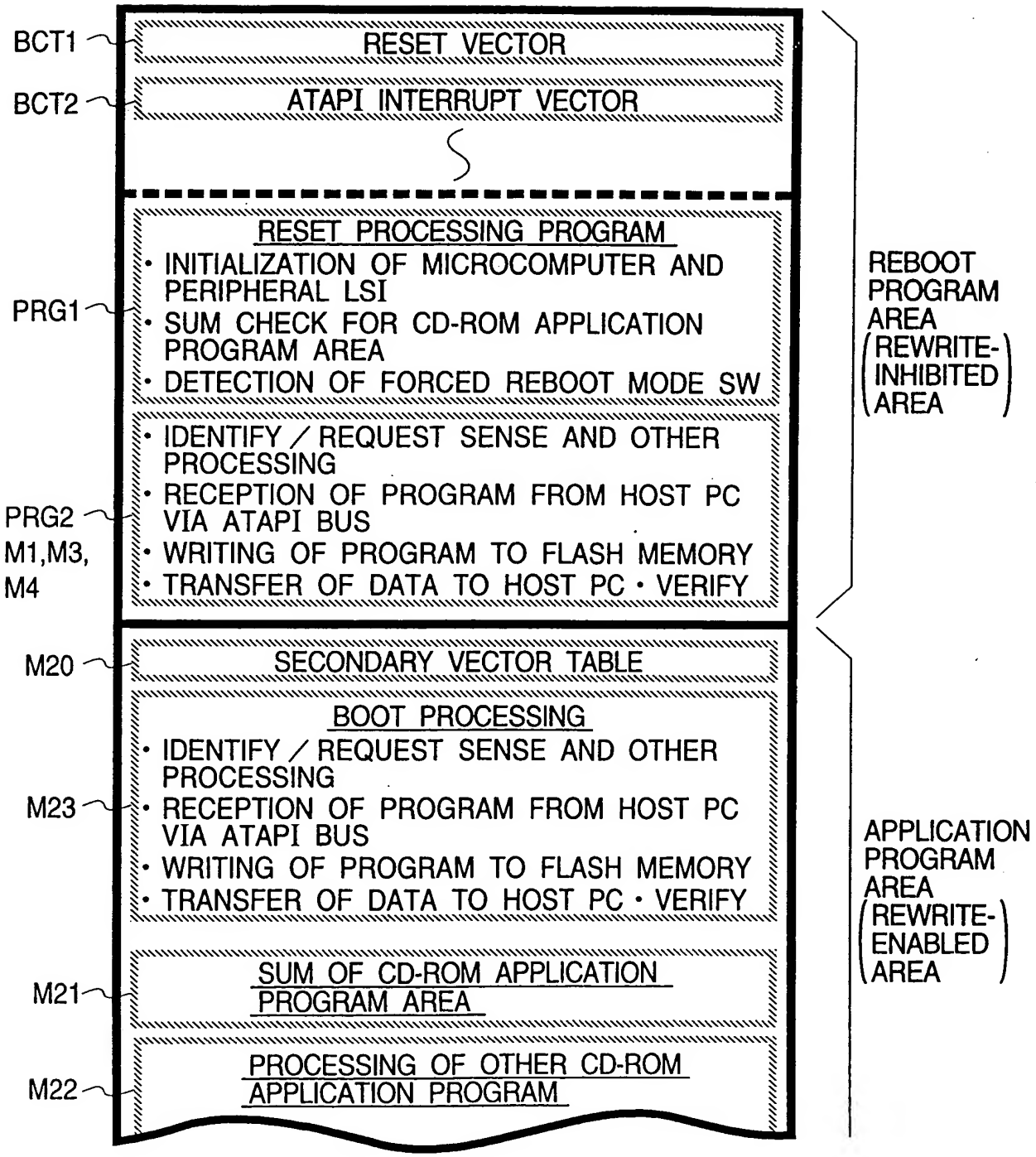

BCT1
RESET VECTOR
BCT2
ATAPI INTERRUPT VECTOR
RESET PROCESSING PROGRAM
PRG1
• INITIALIZATION OF MICROCOMPUTER AND PERIPHERAL LSI
• SUM CHECK FOR CD-ROM APPLICATION PROGRAM AREA
• DETECTION OF FORCED REBOOT MODE SW
PRG2
M1,M3,
M4
• IDENTIFY / REQUEST SENSE AND OTHER PROCESSING
• RECEPTION OF PROGRAM FROM HOST PC VIA ATAPI BUS
• WRITING OF PROGRAM TO FLASH MEMORY
• TRANSFER OF DATA TO HOST PC • VERIFY
REBOOT PROGRAM AREA (REWRITE-INHIBITED AREA)
M20
SECONDARY VECTOR TABLE
BOOT PROCESSING
M23
• IDENTIFY / REQUEST SENSE AND OTHER PROCESSING
• RECEPTION OF PROGRAM FROM HOST PC VIA ATAPI BUS
• WRITING OF PROGRAM TO FLASH MEMORY
• TRANSFER OF DATA TO HOST PC • VERIFY
M21
SUM OF CD-ROM APPLICATION PROGRAM AREA
M22
PROCESSING OF OTHER CD-ROM APPLICATION PROGRAM
APPLICATION PROGRAM AREA (REWRITE-ENABLED AREA)

FIG. 27

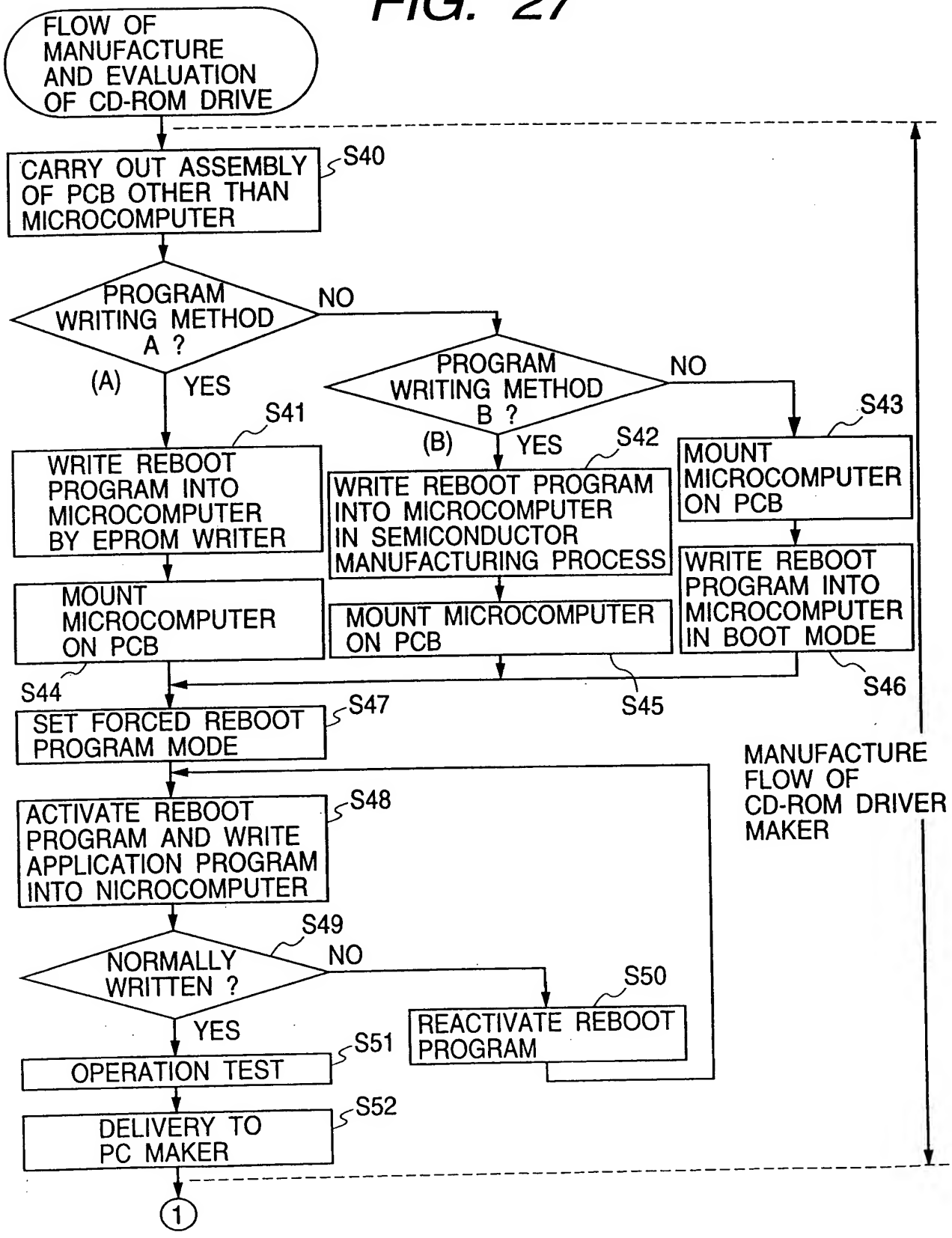

FLOW OF MANUFACTURE AND EVALUATION OF CD-ROM DRIVE
CARRY OUT ASSEMBLY OF PCB OTHER THAN MICROCOMPUTER
S40
PROGRAM WRITING METHOD A ?
NO
(A)
YES
PROGRAM WRITING METHOD B ?
NO
(B)
YES
S41
S42
S43
WRITE REBOOT PROGRAM INTO MICROCOMPUTER BY EPROM WRITER
WRITE REBOOT PROGRAM INTO MICROCOMPUTER IN SEMICONDUCTOR MANUFACTURING PROCESS
MOUNT MICROCOMPUTER ON PCB
MOUNT MICROCOMPUTER ON PCB
WRITE REBOOT PROGRAM INTO MICROCOMPUTER IN BOOT MODE
S44
S45
S46
SET FORCED REBOOT PROGRAM MODE
S47
ACTIVATE REBOOT PROGRAM AND WRITE APPLICATION PROGRAM INTO NICROCOMPUTER
S48
NORMALLY WRITTEN ?
S49
NO
YES
S50
REACTIVATE REBOOT PROGRAM
OPERATION TEST
S51
DELIVERY TO PC MAKER
S52
1
MANUFACTURE FLOW OF CD-ROM DRIVER MAKER

FIG. 28

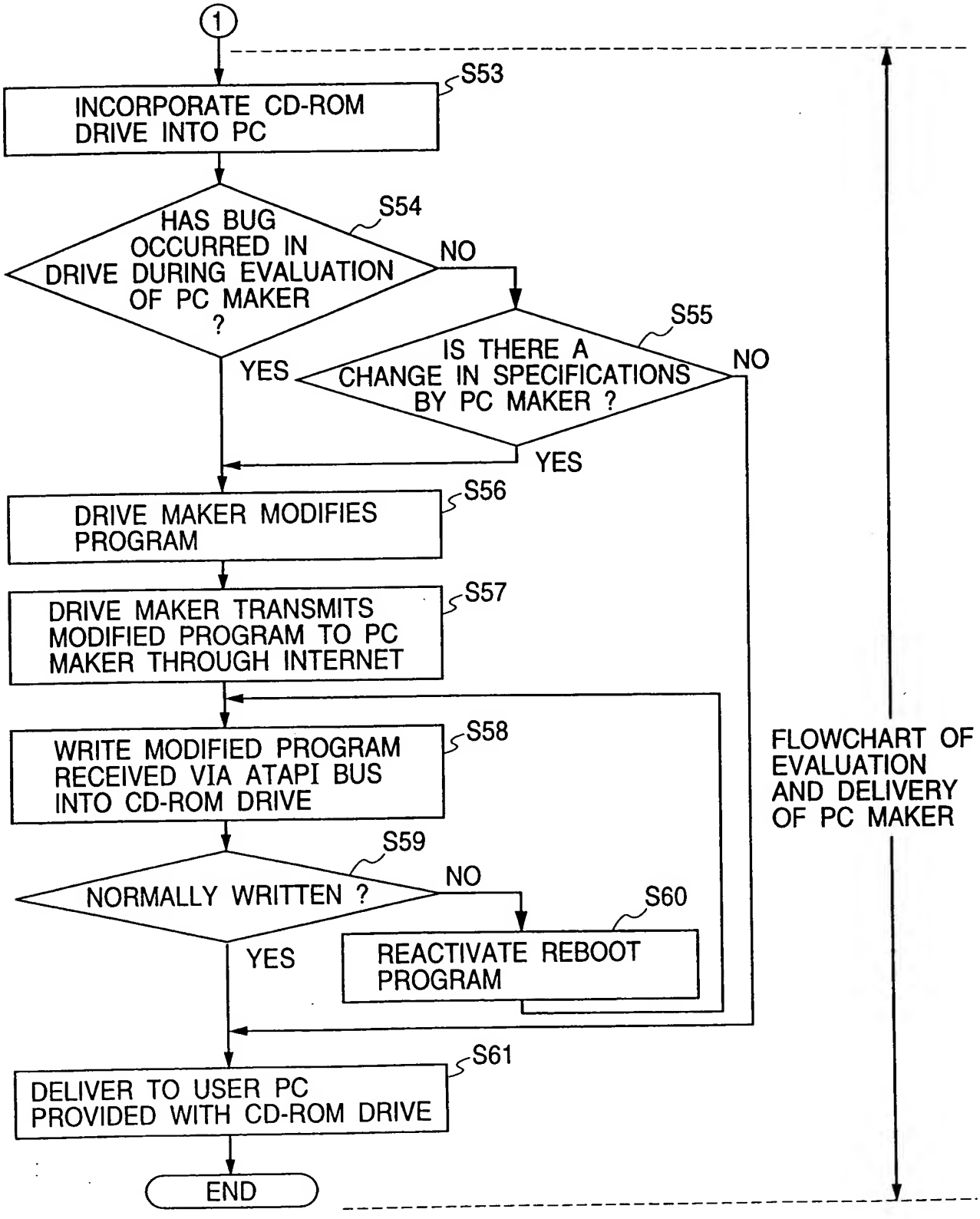

1
INCORPORATE CD-ROM DRIVE INTO PC
S53
HAS BUG OCCURRED IN DRIVE DURING EVALUATION OF PC MAKER ?
S54
NO
YES
IS THERE A CHANGE IN SPECIFICATIONS BY PC MAKER ?
S55
NO
YES
DRIVE MAKER MODIFIES PROGRAM
S56
DRIVE MAKER TRANSMITS MODIFIED PROGRAM TO PC MAKER THROUGH INTERNET
S57
WRITE MODIFIED PROGRAM RECEIVED VIA ATAPI BUS INTO CD-ROM DRIVE
S58
NORMALLY WRITTEN ?
S59
NO
YES
REACTIVATE REBOOT PROGRAM
S60
DELIVER TO USER PC PROVIDED WITH CD-ROM DRIVE
S61
END
FLOWCHART OF EVALUATION AND DELIVERY OF PC MAKER

FIG. 29

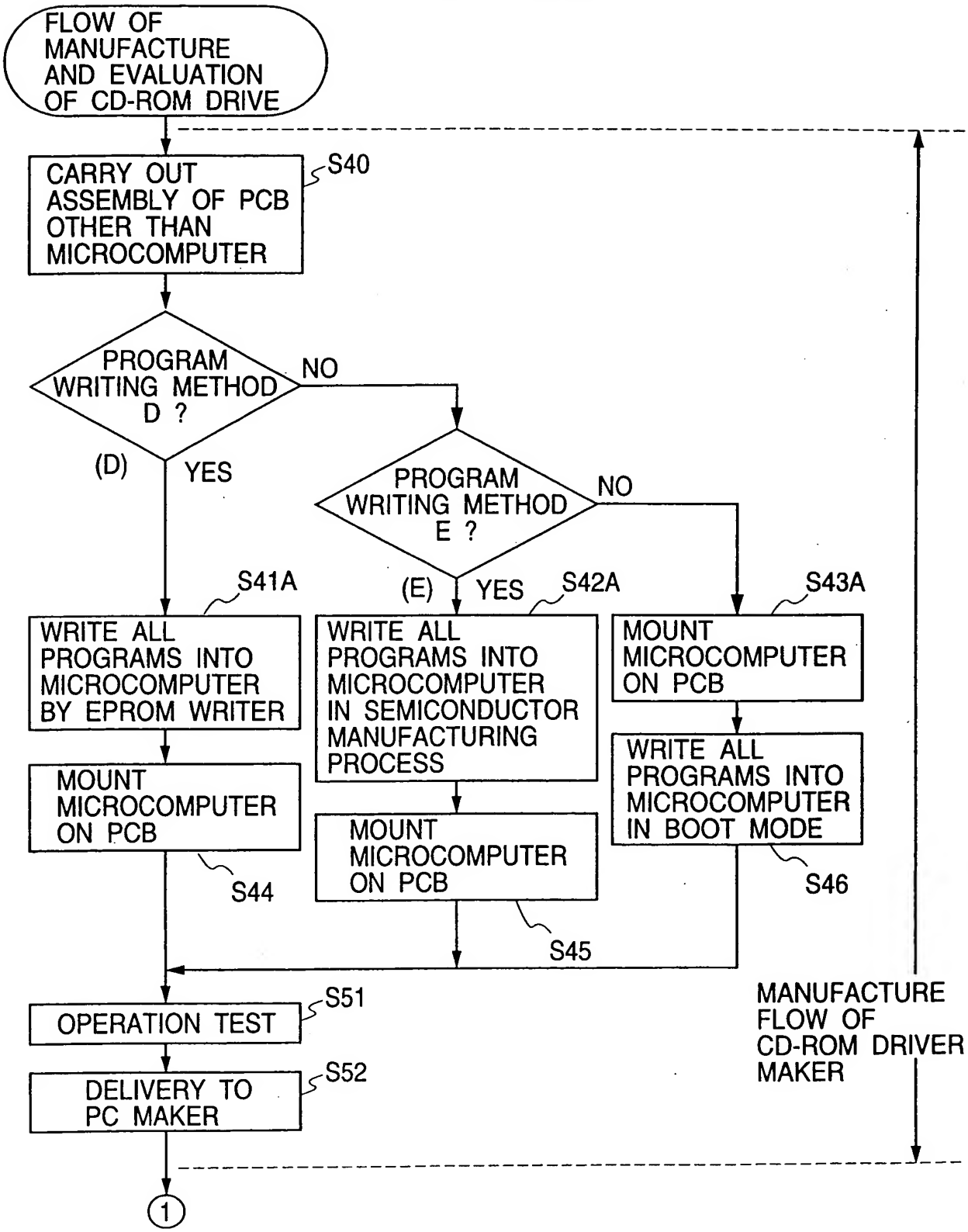

FLOW OF MANUFACTURE AND EVALUATION OF CD-ROM DRIVE
CARRY OUT ASSEMBLY OF PCB OTHER THAN MICROCOMPUTER
S40
PROGRAM WRITING METHOD D ?
NO
(D)
YES
PROGRAM WRITING METHOD E ?
NO
(E)
YES
S41A
S42A
S43A
WRITE ALL PROGRAMS INTO MICROCOMPUTER BY EPROM WRITER
WRITE ALL PROGRAMS INTO MICROCOMPUTER IN SEMICONDUCTOR MANUFACTURING PROCESS
MOUNT MICROCOMPUTER ON PCB
MOUNT MICROCOMPUTER ON PCB
WRITE ALL PROGRAMS INTO MICROCOMPUTER IN BOOT MODE
S44
S45
S46
OPERATION TEST
S51
DELIVERY TO PC MAKER
S52
MANUFACTURE FLOW OF CD-ROM DRIVER MAKER
1

FIG. 30

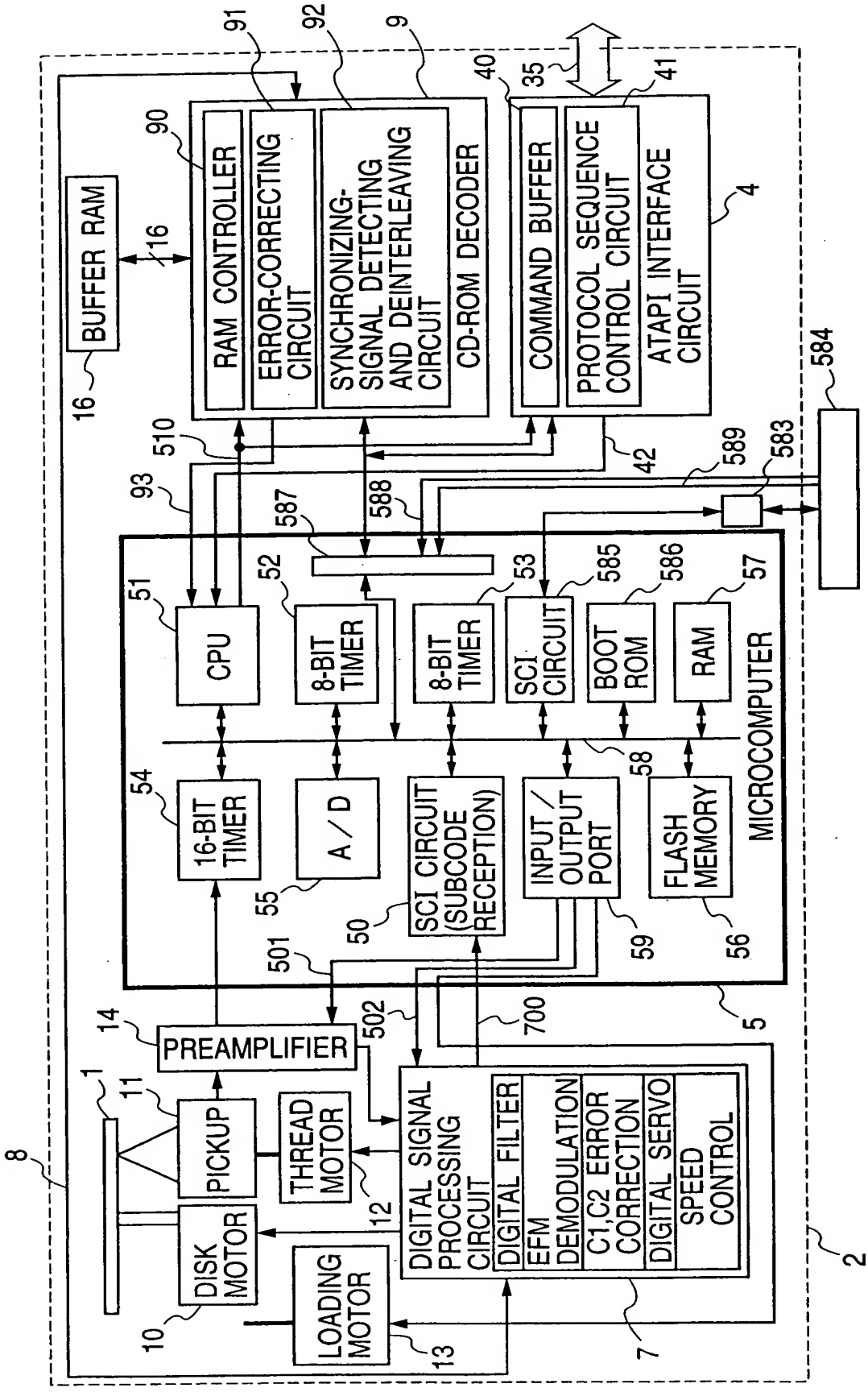
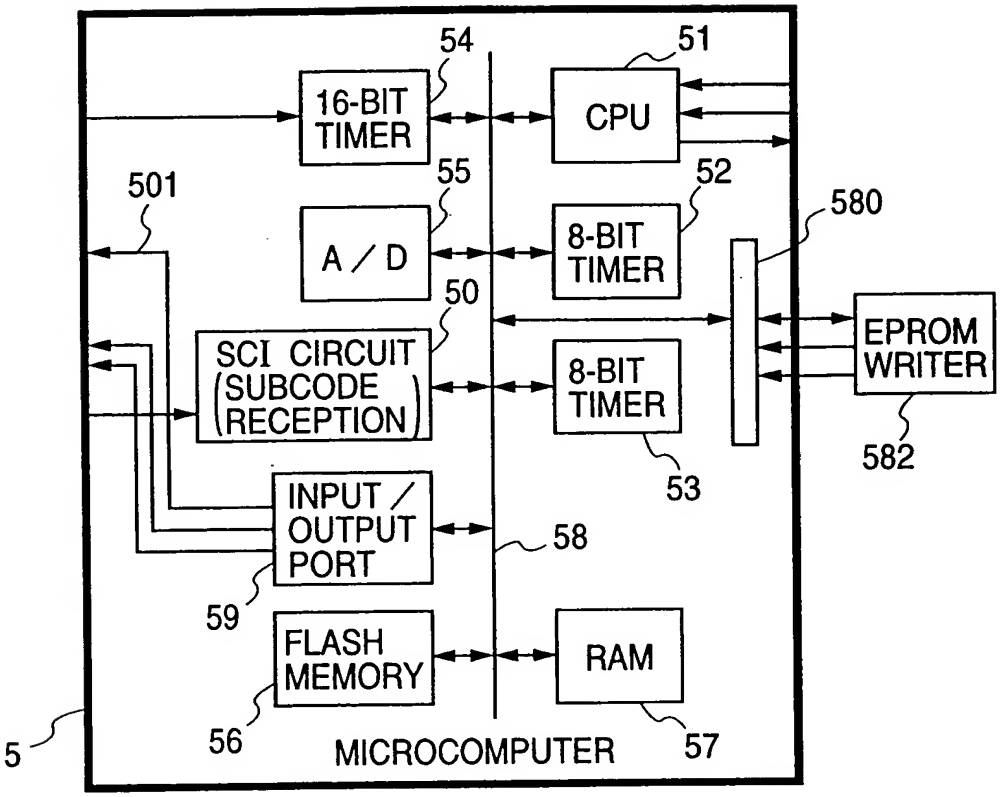

8
1
11
PICKUP
THREAD MOTOR
12
DISK MOTOR
10
LOADING MOTOR
13
14
PREAMPLIFIER
502
DIGITAL SIGNAL PROCESSING CIRCUIT
DIGITAL FILTER
EFM DEMODULATION
C1,C2 ERROR CORRECTION
DIGITAL SERVO
SPEED CONTROL
7
700
5
MICROCOMPUTER
CPU
51
8-BIT TIMER
52
8-BIT TIMER
53
SCI CIRCUIT
585
BOOT ROM
586
RAM
57
16-BIT TIMER
54
A / D
55
SCI CIRCUIT (SUBCODE RECEPTION)
50
INPUT / OUTPUT PORT
59
FLASH MEMORY
56
58
501
587
588
93
510
BUFFER RAM
16
16
90
RAM CONTROLLER
ERROR-CORRECTING CIRCUIT
SYNCHRONIZING-SIGNAL DETECTING AND DEINTERLEAVING CIRCUIT
CD-ROM DECODER
91
92
9
40
35
41
COMMAND BUFFER
PROTOCOL SEQUENCE CONTROL CIRCUIT
ATAPI INTERFACE CIRCUIT
4
42
589
583
584
2

FIG. 31


54
51
16-BIT TIMER
CPU
501
55
52
580
A / D
8-BIT TIMER
50
EPROM WRITER
SCI CIRCUIT (SUBCODE RECEPTION)
8-BIT TIMER
582
53
INPUT / OUTPUT PORT
58
59
FLASH MEMORY
RAM
5
56
MICROCOMPUTER
57